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PARTNERSHIP  
PROJECT 2  
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## ***Physical Layer for cdma2000 Extended Cell High Rate Packet Data Air Interface Specification***

### ***Revision 0***

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## Revision History

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<b>Revision</b>	<b>Description of Changes</b>	<b>Date</b>
Rev 0 v1.0	Initial Publication	January 2011
Rev 0 v1.0	Re-publication to fix some issues in pdf file	September 2011

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**FOREWORD**

1

**(This foreword is not part of this Standard)**

2

This standard was prepared by Technical Specification Group C of the Third Generation Partnership Project 2 (3GPP2). This standard is evolved from and is a companion to the cdma2000<sup>®1</sup> standards. This air interface standard provides Physical Layer part of the extended cell high rate packet data air interface. Other parts of this standard are:

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- Introduction of cdma2000 Extended Cell High Rate Packet Data Air Interface Specification

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- Upper Layers for cdma2000 Extended Cell High Rate Packet Data Air Interface Specification

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<sup>1</sup> “cdma2000<sup>®</sup> is the trademark for the technical nomenclature for certain specifications and standards of the Organizational Partners (OPs) of 3GPP2. Geographically (and as of the date of publication), cdma2000<sup>®</sup> is a registered trademark of the Telecommunications Industry Association (TIA-USA) in the United States.”

**FOREWORD**

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**REFERENCES**

1 The following documents contain provisions, which, through reference in this text,  
 2 constitute provisions of this document. References are either specific (identified by date  
 3 of publication, edition number, version number, etc.) or non-specific. For a specific  
 4 reference, subsequent revisions do not apply. For a non-specific reference, the latest  
 5 version applies. In the case of a reference to a 3GPP2 document, a non-specific  
 6 reference implicitly refers to the latest version of that document in the same Release as  
 7 the present document.

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<sup>2</sup> Editor's Note: The above documents are work in progress and should not be referenced unless and until they are approved and published. Until such time as this Editor's Note is removed, the inclusion of the above documents is for informational purposes only.

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- 20 [26] 3GPP2 X.S0011-E, cdma2000 Wireless IP Network Standard, November 2009.
- 21 [27] 3GPP2 C.S0072-0 v1.0, Mobile Station Equipment Identifier (MEID) Support  
22 for cdma2000 Spread Spectrum Systems, August 2005.
- 23 [28] 3GPP2 C.S0063-B v1.0, cdma2000 High Rate Packet Data Supplemental  
24 Services, May 2010.

25

# 1 PHYSICAL LAYER

## 1.1 xHRPD Subtype 0 Physical Layer Protocol Instance

### 1.1.1 Overview

This document contains the specification for the xHRPD Subtype 0 Physical Layer Protocol. The xHRPD Subtype 0 Physical Layer supports the xHRPD Subtype 0 Access Channel MAC Protocol, the HRPD Default Control Channel MAC Protocol, the HRPD Enhanced (Subtype 1) Control Channel MAC Protocol, xHRPD Subtype 0 and Subtype 1 Forward Traffic Channel MAC Protocols, and the xHRPD Subtype 0 Reverse Traffic Channel MAC Protocol.

### 1.1.2 Primitives and Public Data

#### 1.1.2.1 Commands

This protocol does not define any commands.

#### 1.1.2.2 Return Indications

This protocol returns the following indications:

- *ForwardTrafficCompleted*

#### 1.1.2.3 Public Data

This protocol shall make the following data public:

- Subtype for this protocol

### 1.1.3 Protocol Data Unit

The transmission unit of this protocol is a xHRPD Subtype 0 Physical Layer packet. Each xHRPD Subtype 0 Physical Layer packet contains a MAC Layer packet.

### 1.1.4 Protocol Initialization

#### 1.1.4.1 Protocol Initialization for the InConfiguration Protocol Instance

Upon creation, the InConfiguration instance of this protocol in the access terminal and the access network shall perform the following in the order specified:

- The fall-back values of the attributes for this protocol instance shall be set to the default values specified for each attribute.
- If the InUse instance of this protocol has the same protocol subtype as this InConfiguration protocol instance, then the fall-back values of the attributes defined by the InConfiguration protocol instance shall be set to the values of the corresponding attributes associated with the InUse protocol instance.
- The value for each attribute for this protocol instance shall be set to the fall-back value for that attribute.

- The value of the public data for the InConfiguration protocol instance shall be set to the value of the public data for the InUse protocol instance.

### 1.1.5 Procedures and Messages for the InConfiguration Instance of the Protocol

#### 1.1.5.1 Procedures

This protocol uses the Generic Configuration Protocol (see [1]) to define the processing of the configuration messages.

#### 1.1.5.2 Commit Procedures

The access terminal and the access network shall perform the procedures specified in this section, in the order specified, when directed by the InUse instance of the Session Configuration Protocol to execute the Commit procedures:

- All the public data that are defined by this protocol, but are not defined by the InUse protocol instance shall be added to the public data of the InUse protocol.
- If the InUse instance of this protocol has the same subtype as this protocol instance, then
  - The access terminal and the access network shall set the attribute values associated with the InUse instance of this protocol to the attribute values associated with the InConfiguration instance of this protocol.
  - The access terminal and the access network shall purge the InConfiguration instance of the protocol.
- If the InUse instance of this protocol does not have the same subtype as this protocol instance, then the access network and the access terminal shall perform the following in the order specified:
  - The access terminal and the access network shall set the initial state for the InConfiguration instance of this protocol to the Inactive State.
  - The InConfiguration protocol instance shall become the InUse protocol instance for this Protocol.
- All the public data not defined by this protocol shall be removed from the public data of the InUse protocol.

#### 1.1.5.3 Message Formats

##### 1.1.5.3.1 ConfigurationRequest

The ConfigurationRequest message format is as follows:

Field	Length (bits)
MessageID	8
TransactionID	8

Zero or more instances of the following record

AttributeRecord	Attribute dependent
-----------------	---------------------

- 1 MessageID The sender shall set this field to 0x50.
- 2 TransactionID The sender shall increment this value for each new
- 3 ConfigurationRequest message sent.
- 4 AttributeRecord The format of this record is specified in [1].

5 1.1.5.3.2 ConfigurationResponse

6 The ConfigurationResponse message format is as follows:

Field	Length (bits)
MessageID	8
TransactionID	8

7 Zero or more instances of the following record

AttributeRecord	Attribute dependent
-----------------	---------------------

- 8 MessageID The sender shall set this field to 0x51.
- 9 TransactionID The sender shall set this value to the TransactionID field of the
- 10 corresponding ConfigurationRequest message.
- 11 AttributeRecord An attribute record containing a single attribute value. If this
- 12 message selects a complex attribute, only the ValueID field of the
- 13 complex attribute shall be included in the message. The format of the
- 14 AttributeRecord is given in [1]. The sender shall not include more
- 15 than one attribute record with the same attribute identifier.

<b>Channels</b>	FTC RTC	<b>SLP</b>	Reliable
<b>Addressing</b>	Unicast	<b>Priority</b>	40

17

18 1.1.6 Procedures and Messages for the InUse Instance of the Protocol

19 1.1.6.1 Procedures

20 Procedures for the InUse Instance of the protocol are described in 1.2, 1.3, and 1.4.

1 1.1.6.2 Message Formats

2 1.1.6.2.1 AttributeUpdateRequest

3 The sender sends an AttributeUpdateRequest message to offer an attribute-value for a given  
 4 attribute.

5

Field	Length (bits)
MessageID	8
TransactionID	8

One or more instances of the following record

AttributeRecord	Attribute dependent
-----------------	---------------------

6 MessageID The sender shall set this field to 0x52.

7 TransactionID The sender shall increment this value for each new  
 8 AttributeUpdateRequest message sent.

9 AttributeRecord The format of this record is specified in [1].

10

<b>Channels</b>	FTC RTC	<b>SLP</b>	Reliable
<b>Addressing</b>	unicast	<b>Priority</b>	40

11 1.1.6.2.2 AttributeUpdateAccept

12 The sender sends an AttributeUpdateAccept message in response to an  
 13 AttributeUpdateRequest message to accept the offered attribute values.

14

Field	Length (bits)
MessageID	8
TransactionID	8

15 MessageID The sender shall set this field to 0x53.

16 TransactionID The sender shall set this value to the TransactionID field of the  
 17 corresponding AttributeUpdateRequest message.

18

<b>Channels</b>	FTC RTC	<b>SLP</b>	Reliable
<b>Addressing</b>	unicast	<b>Priority</b>	40

19 1.1.6.2.3 AttributeUpdateReject

20 The access network sends an AttributeUpdateReject message in response to an  
 21 AttributeUpdateRequest message to reject the offered attribute values.

1

<b>Field</b>	<b>Length (bits)</b>
MessageID	8
TransactionID	8

2

MessageID            The access network shall set this field to 0x54.

3

TransactionID        The access network shall set this value to the TransactionID field of  
the corresponding AttributeUpdateRequest message.

4

<b>Channels</b>	FTC	<b>SLP</b>	Reliable
<b>Addressing</b>	unicast	<b>Priority</b>	40

5

### 1.1.6.3 Interface to Other Protocols

6

#### 1.1.6.3.1 Commands

7

These protocols do not issue any commands.

8

#### 1.1.6.3.2 Indications

9

These protocols do not register to receive any indications

10

### 1.1.7 Configuration Attributes

11

No configuration attributes are defined for these protocols.

12

### 1.1.8 Protocol Numeric Constants

13

<b>Constant</b>	<b>Meaning</b>	<b>Value</b>
N <sub>PHYPTYPE</sub>	Type field for this protocol	Table 1.5.4-1 of [5]
N <sub>xHRPDSOPHYP</sub>	Subtype field for this protocol	0x0000

14

15

### 1.1.9 Session State Information

16

This protocol does not define any parameter record to be included in a Session State Information record (see [1]).

17

18

19

## 1.2 Physical Layer Packets

### 1.2.1 Overview

The transmission unit of the physical layer is a physical layer packet. A physical layer packet on the forward link can be of length 128, 256, 512, 768, 1024, 2048, 3072, 4096, or 5120 bits. The reverse link supports two types of physical layer packets: Voice packet and Data packet. The Voice packet can be of length 48, 96 or 192 bits and the Data packet can be of length 192, 256, 384, 512 or 768 bits. The Voice packets are sent in a single 20 ms frame whereas the Data packet can be sent over multiple 20 ms frames. The format of the physical layer packet depends upon the channel on which it is transmitted. A physical layer packet carries one MAC layer packet.

### 1.2.2 Physical Layer Packet Formats

#### 1.2.2.1 Control Channel Physical Layer Packet Format

The length of a Control Channel physical layer packet shall be 128, 256, 512, or 1024 bits. Each Control Channel physical layer packet shall carry one Control Channel MAC layer packet. The 1024-bit Control Channel physical layer packets shall use the following format:

Field	Length (bits)
MAC Layer Packet	1,002
FCS	16
TAIL	6

MAC Layer Packet - MAC layer packet from the Control Channel MAC Protocol.

FCS - Frame check sequence (see 1.2.4).

TAIL - Encoder tail bits. This field shall be set to all '0's.

All other Control Channel physical layer packets shall use the following format:

Field	Length (bits)
MAC Layer Packet	98, 226, or 482
FCS	24
TAIL	6

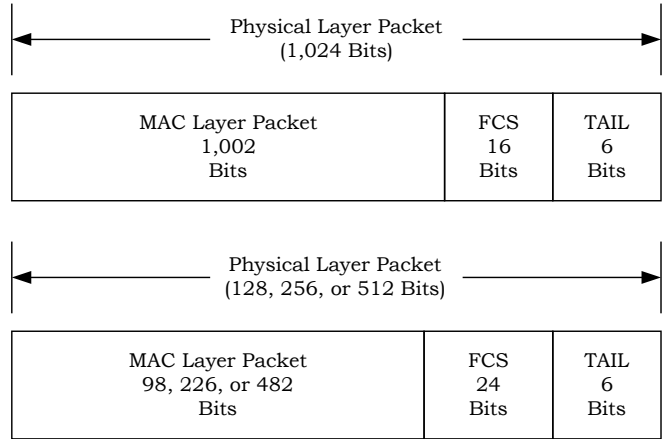
MAC Layer Packet - MAC layer packet from the Control Channel MAC Protocol.

FCS - Frame check sequence (see 1.2.4).

TAIL - Encoder tail bits. This field shall be set to all '0's.

Figure 1.2.2.1-1 illustrates the valid formats for the Control Channel physical layer packets.

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**Figure 1.2.2.1-1. Physical Layer Packet Formats for the Control Channel**

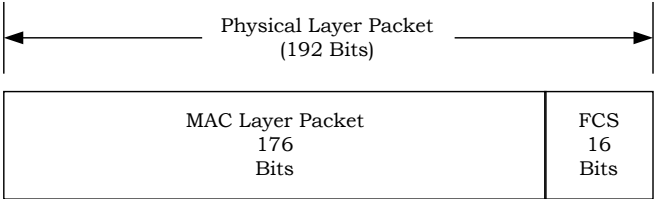
1.2.2.2 Access Channel Physical Layer Packet Format

The length of an Access Channel physical layer packet shall be 192 bits. Each Access Channel physical layer packet shall carry one Access Channel MAC layer packet. Access Channel physical layer packets shall use the following format:

Field	Length (bits)
MAC Layer Packet	176
FCS	16

- MAC Layer Packet - MAC layer packet from the Access Channel MAC Protocol.
- FCS - Frame check sequence (see 1.2.4).

Figure 1.2.2.2-1 illustrates the format of the Access Channel physical layer packets.



**Figure 1.2.2.2-1. Physical Layer Packet Format for the Access Channel**

1.2.2.3 Forward Traffic Channel Physical Layer Packet Format

The length of a Forward Traffic Channel physical layer packet shall be 128, 256, 512, 1024, 2048, 3072, 4096, or 5120 bits. A Forward Traffic Channel physical layer packet shall carry one Forward Traffic Channel MAC layer packet addressed to one or more access terminals. Forward Traffic Channel physical layer packets shall use the following format:



1

**Table 1.2.2.4-1. Reverse Traffic Channel Physical Layer Packet Types and Sizes**

<b>Packet Type</b>	<b>Packet Size (bits)</b>	<b>MAC Layer Packet (bits)</b>	<b>FCS (bits)</b>	<b>Tail (bits)</b>
Voice	48	40	8	0
Voice	96	80	16	0
Voice	192	171	11	10
Data	192	176	16	0
Data	192	166	16	10
Data	256	234	16	6
Data	384	362	16	6
Data	512	490	16	6
Data	768	746	16	6

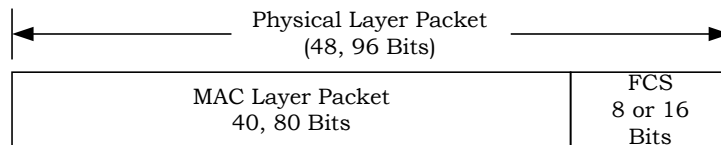
2

3 MAC Layer Packet - MAC layer packet from the Reverse Traffic Channel MAC  
4 Protocol.

5 FCS - Frame check sequence (see 1.2.4).

6 TAIL - Encoder tail bits. This field shall be set to all '0's.

7 Figure 1.2.2.4-1 to Figure 1.2.2.4-3 illustrate the formats of different Reverse Traffic  
8 Channel physical layer packets.

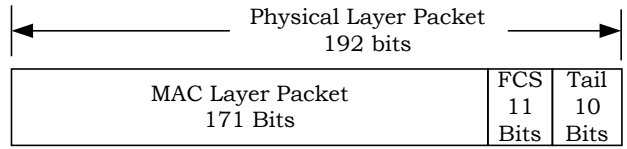


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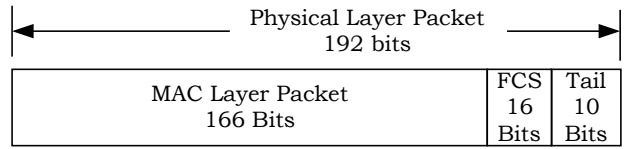
10 **Figure 1.2.2.4-1. Physical Layer Packet Format for the 48-bit and 96-bit Voice Packet**  
11 **on Reverse Traffic Channel**

12

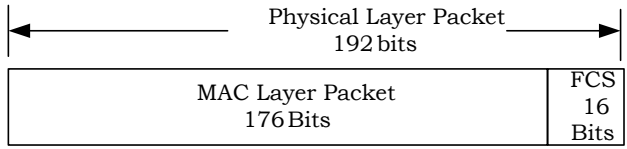
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(a) Format of 192-bit Voice Packet

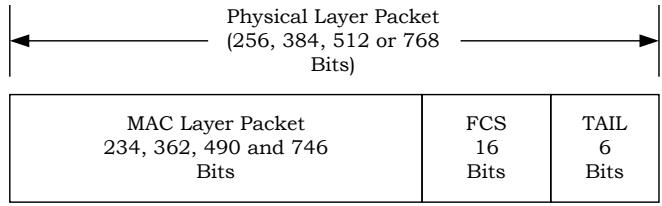


(b) Format of 192-bit Data Packet at 9.6 kbps



(c) Format of 192-bit Data Packet at 4.8 and 2.4 kbps

**Figure 1.2.2.4-2. Physical Layer Packet Format for the 192-bit Voice and Data Packet on Reverse Traffic Channel**



**Figure 1.2.2.4-3. Physical Layer Packet Format for the Large Size (>192 bits) Data Packet on Reverse Traffic Channel**

1.2.3 Bit Transmission Order

Each field of the physical layer packets shall be transmitted in sequence such that the most significant bit (MSB) is transmitted first and the least significant bit (LSB) is transmitted last. The MSB is the left-most bit in the figures of the document.

1.2.4 Computation of the FCS Bits

The FCS computation described here shall be used for computing the FCS field in the Control Channel physical layer packets, the Forward Traffic Channel physical layer packets, the Access Channel physical layer packets, and the Reverse Traffic Channel physical layer packets.

The 16-bit FCS on the Control Channel shall be a CRC calculated using the standard CRC-CCITT generator polynomial:

1 
$$g(x) = x^{16} + x^{12} + x^5 + 1.$$

2 The 24-bit FCS shall be a CRC calculated using the standard CRC-CCITT generator  
3 polynomial:

4 
$$g(x) = x^{24} + x^{23} + x^6 + x^5 + x + 1.$$

5 The 8-bit FCS on the Reverse Traffic (Voice) Channel shall be a CRC calculated using the  
6 generator polynomial:

7 
$$g(x) = x^8 + x^7 + x^4 + x^3 + x + 1.$$

8 The 11-bit FCS on the Reverse Traffic (Voice) Channel shall be a CRC calculated using the  
9 generator polynomial:

10 
$$g(x) = x^{11} + x^9 + x^8 + x^7 + x^2 + 1.$$

11 The 16-bit FCS on the Reverse Traffic (Voice) Channel shall be a CRC calculated using the  
12 generator polynomial:

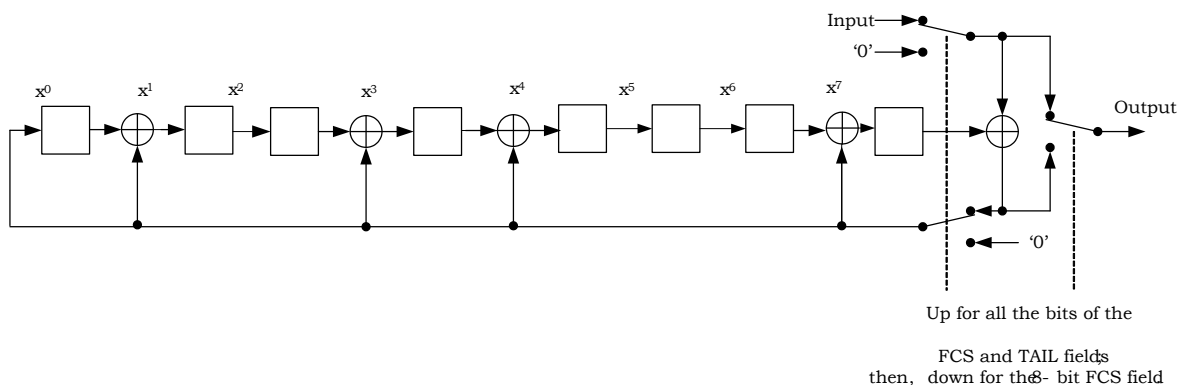
13 
$$g(x) = x^{16} + x^{12} + x^5 + 1.$$

14 The 16-bit FCS on the Reverse Traffic (Data) Channel and Access Channel shall be a CRC  
15 calculated using the generator polynomial:

16 
$$g(x) = x^{16} + x^{15} + x^{14} + x^{11} + x^6 + x^5 + x^2 + x + 1.$$

17 The 8-bit FCS shall be equal to the value computed according to the following procedure as  
18 shown in Figure 1.2.4-1:

- 19
- All shift-register elements shall be initialized to '0's.
  - The switches shall be set in the up position.
  - The register shall be clocked once for each bit of the physical layer packet except for the  
22 FCS and TAIL fields. The physical layer packet shall be read from MSB to LSB.
  - The switches shall be set in the down position so that the output is a modulo-2 addition  
23 with a '0' and the successive shift-register inputs are '0's.
  - The register shall be clocked an additional 8 times for the 8 FCS bits.
  - The output bits constitute all fields except the TAIL field of the physical layer.
- 26



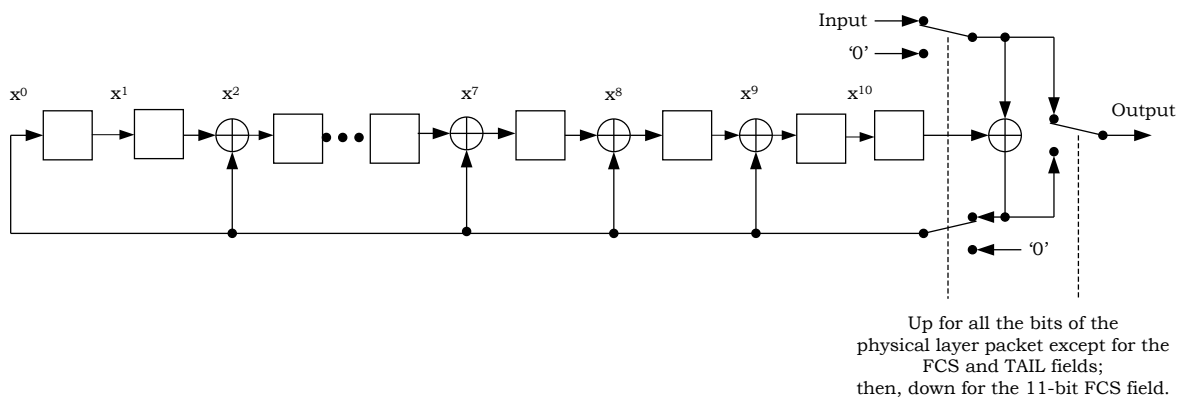
27

28

**Figure 1.2.4-1. 8-bit FCS Computation for the Physical Layer Packet**

1 The 11-bit FCS shall be equal to the value computed according to the following procedure  
 2 as shown in Figure 1.2.4-2:

- 3 • All shift-register elements shall be initialized to '0's.
- 4 • The switches shall be set in the up position.
- 5 • The register shall be clocked once for each bit of the physical layer packet except for the  
 6 FCS and TAIL fields. The physical layer packet shall be read from MSB to LSB.
- 7 • The switches shall be set in the down position so that the output is a modulo-2 addition  
 8 with a '0' and the successive shift-register inputs are '0's.
- 9 • The register shall be clocked an additional 11 times for the 11 FCS bits.
- 10 • The output bits constitute all fields except the TAIL field of the physical layer.

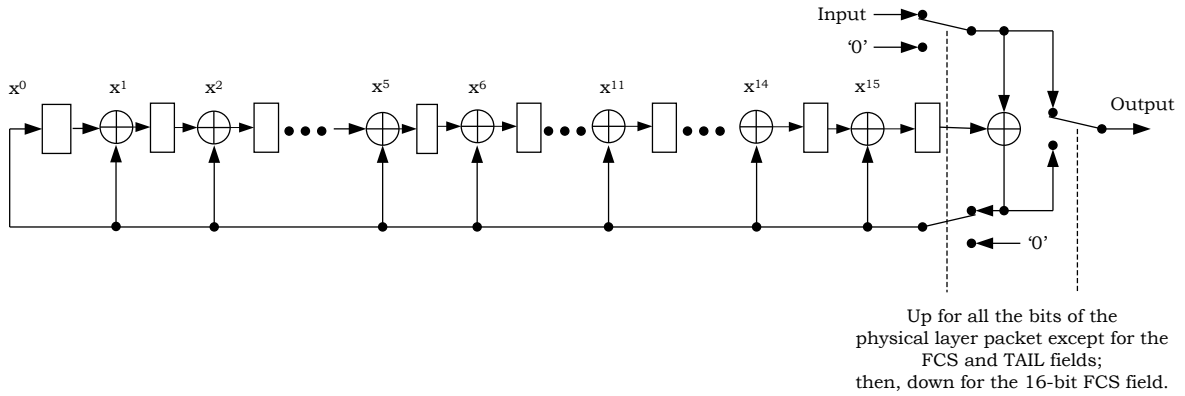


11

12 **Figure 1.2.4-2. 11-bit FCS Computation for the Physical Layer Packet**

13 The 16-bit FCS for the reverse Data packet shall be equal to the value computed according  
 14 to the following procedure as shown in Figure 1.2.4-3:

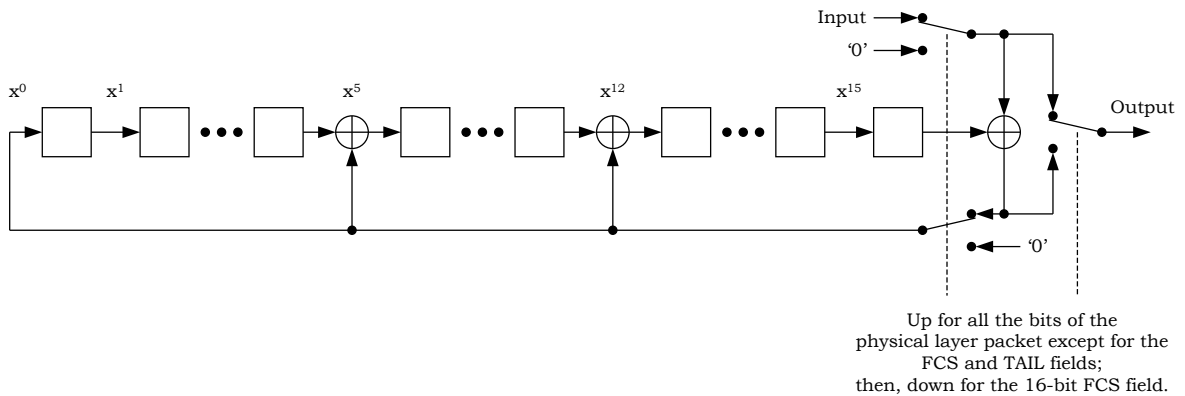
- 15 • All shift-register elements shall be initialized to '0's.
- 16 • The switches shall be set in the up position.
- 17 • The register shall be clocked once for each bit of the physical layer packet except for the  
 18 FCS and TAIL fields. The physical layer packet shall be read from MSB to LSB.
- 19 • The switches shall be set in the down position so that the output is a modulo-2 addition  
 20 with a '0' and the successive shift-register inputs are '0's.
- 21 • The register shall be clocked an additional 16 times for the 16 FCS bits.
- 22 • The output bits constitute all fields except the TAIL field of the physical layer.



**Figure 1.2.4-3. 16-bit FCS Computation for the Reverse Data Packet**

The 16-bit FCS for the Control Channel packet and the 96-bit Reverse Traffic Channel Voice packet shall be equal to the value computed according to the following procedure as shown in Figure 1.2.4-4:

- All shift-register elements shall be initialized to '0's.
- The switches shall be set in the up position.
- The register shall be clocked once for each bit of the physical layer packet except for the FCS and TAIL fields. The physical layer packet shall be read from MSB to LSB.
- The switches shall be set in the down position so that the output is a modulo-2 addition with a '0' and the successive shift-register inputs are '0's.
- The register shall be clocked an additional 16 times for the 16 FCS bits.
- The output bits constitute all fields except the TAIL field of the physical layer.

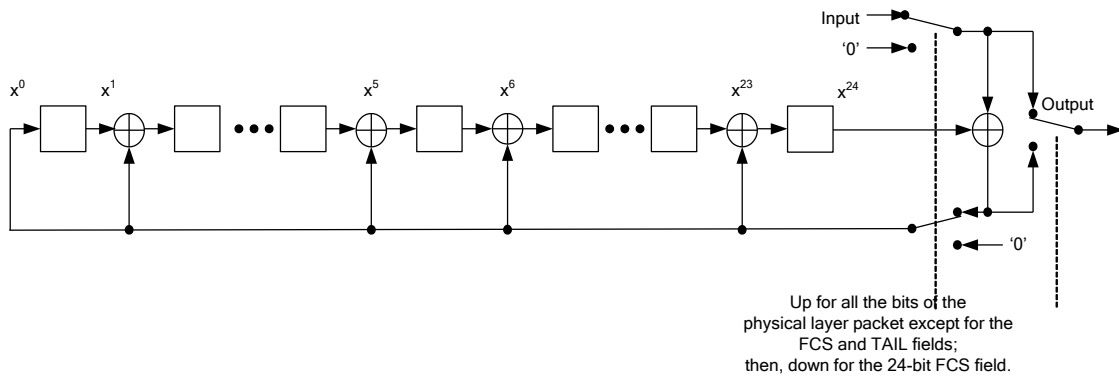


**Figure 1.2.4-4. 16-bit FCS Computation for Control Channel Packet and 96-bit Reverse Voice packet**

The 24-bit FCS shall be equal to the value computed according to the following procedure as shown in Figure 1.2.4-5:

- All shift-register elements shall be initialized to '0's.
- The switches shall be set in the up position.

- 1 • The register shall be clocked once for each bit of the physical layer packet except for the
- 2 FCS and TAIL fields. The physical layer packet shall be read from MSB to LSB.
- 3 • The switches shall be set in the down position so that the output is a modulo-2 addition
- 4 with a '0' and the successive shift-register inputs are '0's.
- 5 • The register shall be clocked an additional 24 times for the 24 FCS bits.
- 6 • The output bits constitute all fields except the TAIL field of the physical layer packets.



7

**Figure 1.2.4-5. 24-bit FCS Computation for the Physical Layer Packet**

8

9

10

### 1.3 Access Terminal Requirements

This section defines requirements specific to access terminal equipment and operation.

#### 1.3.1 Transmitter

##### 1.3.1.1 Frequency Parameters

The access terminal shall meet the requirements in the current version of [23].

##### 1.3.1.1.1 Frequency Tolerance

The access terminal shall meet the requirements in the current version of [13].

##### 1.3.1.2 Power Output Characteristics

All power levels are referenced to the access terminal antenna connector unless otherwise specified.

##### 1.3.1.2.1 Output Power Requirements of Reverse Channels

###### 1.3.1.2.1.1 Access Channel Output Power

When transmitting over the Access Channel, the access terminal transmits Access Probes until the access attempt succeeds or ends. When the access terminal is transmitting the Access Channel, the access terminal shall control the mean output power as specified in the Access Channel MAC Protocol (see [8]).

###### 1.3.1.2.1.2 Reverse Traffic Channel Output Power

When the access terminal is transmitting the Reverse Traffic Channel, the access terminal shall control the mean output power using a combination of closed-loop power control, open-loop power control, and the rules specified by the Reverse Traffic Channel MAC Protocol (see [8]).

###### 1.3.1.2.2 Maximum Output Power

The access terminal shall meet the requirements in the current version of [13].

###### 1.3.1.2.3 Output Power Limits

###### 1.3.1.2.3.1 Minimum Controlled Output Power

The access terminal shall meet the requirements in the current version of [13].

###### 1.3.1.2.3.2 Standby Output Power

The access terminal shall disable its transmitter except when it is instructed by a MAC protocol to transmit. When the transmitter is disabled, the output noise power spectral density of the access terminal shall be less than  $-61$  dBm/1 MHz for all frequencies within the transmit bands that the access terminal supports.

1 1.3.1.2.4 Controlled Output Power

2 The access terminal shall provide two independent means for output power adjustment: an  
3 open-loop estimation performed by the access terminal and a closed-loop correction  
4 involving both the access terminal and the access network. Accuracy requirements on the  
5 controlled range of mean output power need not apply for the following three cases:

- 6 • Mean output power levels exceeding the minimum ERP/EIRP at the maximum output  
7 power for the corresponding access terminal class;
- 8 • Mean output power levels less than the minimum controlled output power (see  
9 1.3.1.2.3.1); or
- 10 • Mean input power levels exceeding  $-25$  dBm within the 1.23-MHz bandwidth.

11 1.3.1.2.4.1 Estimated Open-Loop Output Power

12 Open-loop operation shall be based on the power of the received Forward Pilot Channel (see  
13 1.4.1.3.2.1).

14 The nominal access probe structure and its transmit power requirements are defined as  
15 part of the Access Channel MAC Protocol. The output power of the preamble and data  
16 portion of the access probe are the same.

17 Once instructed by the Reverse Traffic Channel MAC Protocol, the access terminal initiates  
18 Reverse Traffic Channel transmission. The initial mean output power of the Reverse Traffic  
19 Channel shall be equal to the mean output power at the end of the last Access Channel  
20 probe minus the difference in the forward link mean received signal power from the end of  
21 the last Access Channel probe to the start of the Reverse Traffic Channel transmission.

22 The subsequent mean output power of reverse link transmission shall be the mean output  
23 power of the last Access Channel probe minus a function of the difference in the forward  
24 link mean received signal power from the end of the last Access Channel probe to the  
25 current Reverse Traffic Channel transmission, plus closed loop corrections as specified in  
26 1.3.1.2.4.2.

27 The accuracy of the incremental adjustment to the mean output power, as dictated by the  
28 Access Channel MAC Protocol and the Reverse Traffic Channel MAC Protocol, shall be  
29  $\pm 0.5$  dB or 20% of the change in dB, whichever is greater.

30 1.3.1.2.4.2 Closed-Loop Output Power

31 For closed-loop correction (with respect to the open-loop estimate), the access terminal  
32 shall adjust the mean output power level in response to each power-control bit received on  
33 the Reverse Power Control (RPC) Channel.

34 The nominal change in mean output power level per single power-control bit shall be set  
35 according to the RPCStep, which is public data of the Reverse Traffic Channel MAC  
36 Protocol.

37 For the 1.0 dB step size, the change in mean output power level per power-control bit shall  
38 be within  $\pm 0.5$  dB of the nominal value (1 dB), and the change in mean output power level  
39 per 10 power-control bits of the same sign shall be within  $\pm 2.0$  dB of 10 times the nominal

1 change (10 dB). For the 0.5 dB step size, the change in mean output power level per power-  
2 control bit shall be within  $\pm 0.3$  dB of the nominal value (0.5 dB), and the change in mean  
3 output power level per 20 power-control bits of the same sign shall be within  $\pm 2.5$  dB of 20  
4 times the nominal change (10 dB). For the 1.5 dB step size, the change in mean output  
5 power level per power-control bit shall be within  $\pm 0.5$  dB of the nominal value (1.5 dB), and  
6 the change in mean output power level per 10 power-control bits of the same sign shall be  
7 within  $\pm 3.0$  dB of 10 times the nominal change (15 dB). For the 2.0 dB step size, the  
8 change in mean output power level per power-control bit shall be within  $\pm 0.5$  dB of the  
9 nominal value (2.0 dB), and the change in mean output power level per 10 power-control  
10 bits of the same sign shall be within  $\pm 4.0$  dB of 10 times the nominal change (20 dB). A '0'  
11 power-control bit requires the access terminal to increase transmit power, and a '1' power-  
12 control bit requires the access terminal to decrease transmit power. The access terminal  
13 shall provide a closed-loop adjustment range greater than  $\pm 24$  dB around its open-loop  
14 estimate.

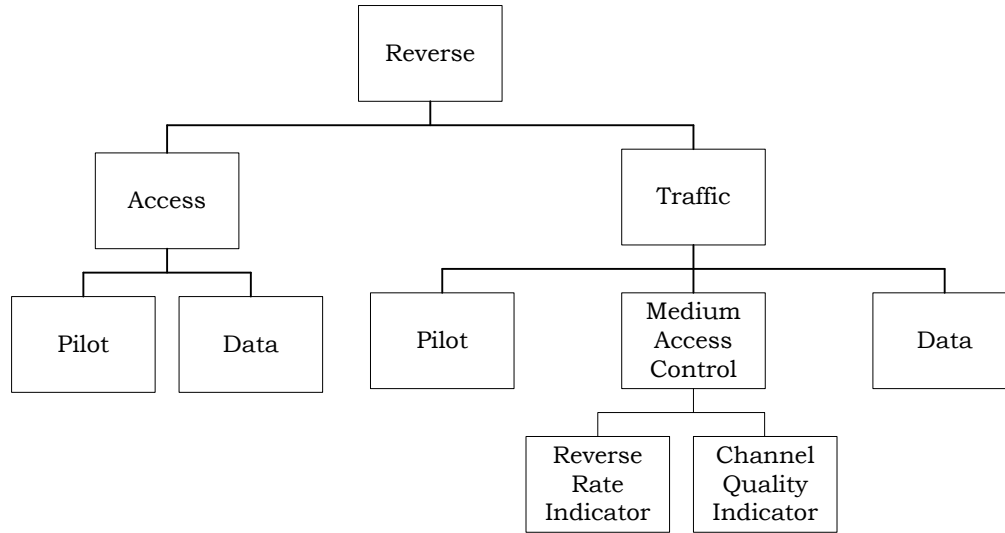
### 15 1.3.1.3 Modulation Characteristics

#### 16 1.3.1.3.1 Reverse Channel Structure

17 The reverse link employs frequency division multiplexing of users using narrowband  
18 frequency channels. A 1.25 MHz block of reverse link spectrum is divided into 192  
19 narrowband frequency channels, each with bandwidth of 6.4 kHz. Users are assigned 6.4  
20 kHz channel or 12.8 kHz channel that consists of 2 consecutive 6.4 kHz channels,  
21 depending primarily on the re-use pattern, channel availability and system load.

22 Reverse Channel consists of the Access Channel and the Reverse Traffic Channel. The  
23 Access Channel shall consist of a Pilot Channel and a Data Channel, and shall occupy 6.4  
24 kHz narrowband frequency channel. The Reverse Traffic Channel shall consist of a Data  
25 Channel, a Pilot Channel, a Reverse Rate Indicator (RRI) Channel and a Channel Quality  
26 Indicator (CQI) Channel. The Pilot Channel is used by the demodulator for phase/gain  
27 estimation and tracking purpose. The CQI Channel is used by the access terminal to  
28 indicate to the access network the data rate it is able to receive on the forward link, while  
29 the RRI Channel is used to indicate the data rate it transmits on the Reverse Traffic  
30 Channel. The CQI and RRI Channels make up the Media Access Control (MAC) channel.  
31 The Data, Pilot, RRI and CQI channels are time division multiplexed (TDM) within a Reverse  
32 Traffic Frame structure (see Figure 1.3.1.3.1-2 and Figure 1.3.1.3.1-3). Reverse Traffic  
33 Channel from an access terminal shall occupy 6.4 kHz or 12.8 kHz narrowband frequency  
34 channel.

35 Figure 1.3.1.3.1-1 shows the reverse channel structure.



**Figure 1.3.1.3.1-1. Reverse Channel Structure**

A frame is the basic transmit time unit on the Reverse Channel. A Reverse Channel frame shall be 20 ms in duration. The Reverse Traffic Channel frame shall carry pilot, data and MAC (CQI and RRI) symbols. The MAC symbols shall be replaced by additional pilot symbols on the Access frame. Each symbol in the frame shall be of equal duration and transmitted at the same power level. The number of symbols in each frame depends on the assigned bandwidth as shown in Table 1.3.1.3.1-1.

**Table 1.3.1.3.1-1. Symbol Numerology Table as a Function of Channel Assignment**

Frequency Assignment	Symbol Rate (kHz)	Number of Symbols per Frame	Number of Data Symbols per Frame	Number of Pilot Symbols per Frame	Number of RRI Symbols per Frame	Number of CQI Symbols per Frame
6.4 kHz ch	5.6	112	94	14	2	2
12.8 kHz ch	11.2	224	188	28	4	4

With 6.4 kHz channel assignment, a 20 ms frame shall consist of 112 modulation symbols which corresponds to 5.6 kbaud symbol rate. The 112 complex symbols shall modulate a root raised-cosine pulse with 14.286% excess bandwidth, so the bandwidth occupied by the transmitted waveform is 6.4 kHz. The 112 modulation symbols shall be arranged within a 20 ms frame as shown in Figure 1.3.1.3.1-2. The 14 pilot symbols shall be evenly distributed within a frame. The symbol indices of these pilot symbols shall satisfy

$$(i-4) \bmod 8 = 0$$

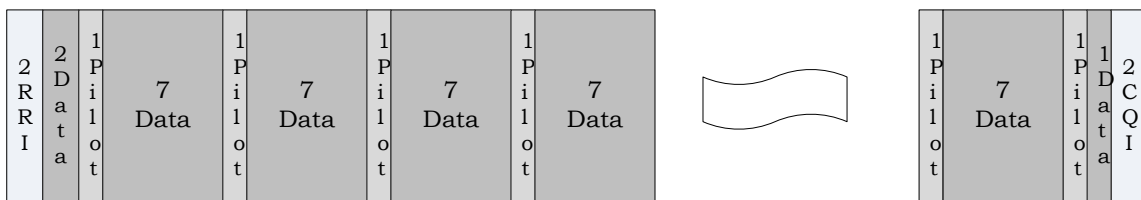
where  $i=0$  to 111 is the symbol index within a frame for 6.4 kHz channel assignment. 2 RRI symbols shall be placed at the beginning of a frame, while 2 CQI symbols shall be placed at the end of a frame. The rest 94 symbols shall be the data symbols.

1 With 12.8 kHz channel assignment, a 20 ms frame shall consist of twice as many symbols  
 2 for Pilot, Data, CQI and RRI channel as with 6.4 kHz channel assignment, as shown in  
 3 Figure 1.3.1.3.1-3. The pilot symbol location indices shall satisfy

4 
$$(i-4) \bmod 8 = 0$$

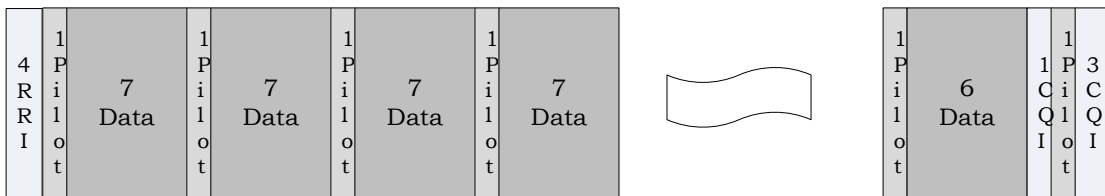
5 where  $i=0$  to 223 is the symbol index within a frame for 12.8 kHz channel assignment. 4  
 6 RRI symbols shall be placed at the beginning of a frame, while 4 CQI symbols shall be  
 7 placed at symbol indices  $i=219, 221, 222, 223$  as the 220<sup>th</sup> symbol is taken by a pilot. The  
 8 rest 188 symbols shall be the data symbols.

9 Access Channel frame shall have the same structure as Reverse Traffic Channel frame  
 10 except all the RRI and CQI symbols shall be replaced by Pilot symbols.



12 **Figure 1.3.1.3.1-2. 20-ms Frame Structure for 6.4 kHz Channel Assignment**

13 (Symbol Rate 5.6 kbaud. Not drawn to scale.)



15 **Figure 1.3.1.3.1-3. 20-ms Frame Structure for 12.8 kHz Channel Assignment**

16 (Symbol Rate 11.2 kbaud. Not drawn to scale.)

17

18

19 When an access terminal has no data to send, it shall send special NULL frame. The NULL  
 20 frame shall consist of all the pilots and MAC (RRI and CQI) symbols for maintaining the  
 21 link and approximately 1/3 of the data symbols in a normal frame. In case of 6.4 kHz  
 22 channel assignment, predetermined 16 symbols shall be transmitted at the data symbol  
 23 positions from the beginning of a frame and another 16 symbols shall be transmitted at the  
 24 last 16 data symbol positions at the end of a frame. In case of 12.8 kHz channel  
 25 assignment, predetermined 32 symbols shall be transmitted at the data symbol positions  
 26 from the beginning of a frame and another 32 symbols shall be transmitted at the last 32  
 27 data symbol positions at the end of a frame. During the other data symbols period the  
 28 transmission shall be gated off for both 1 and 2 channel cases. The 16 or 32 data symbols  
 29 transmitted at the beginning and at the end of a NULL frame shall be alternating binary '0's  
 30 and binary '1's starting with binary '0'. These data symbols shall be BPSK modulated and  
 31 sent on the Q branch. The NULL frame shall be transmitted at the same power level as a  
 32 regular 2.4 kbps data rate frame.

## 1.3.1.3.1.1 Transmit Format and Modulation Parameters

The reverse channel transmit format defines how a physical layer packet shall be transmitted. It is defined by an ordered 3-tuple:

- Bandwidth assigned in units of 6.4 kHz
  - Either 1 or 2 . This is negotiated during the call setup process, depending on an access terminal's transmit power capability, channel condition as well as system load.
- Transmit duration, i.e., number of 20 ms frames needed to transmit a physical layer packet
  - Either one or multiple frames.
- Packet size
  - Physical layer packet size as specified in Table 1.2.2.4-1.

Given the duration and packet size, the transmit data rate is uniquely determined.

Table 1.3.1.3.1.1-1 lists all the transmit formats supported on the reverse channel. Table 1.3.1.3.1.1-2 provides the modulation parameters for these supported formats.

For each of the 2.4 kbps, 4.8 kbps and 9.6 kbps data rates, there are two transmit formats with the same number of narrowband channels, RRI bits and pilot pattern. This ambiguity can be resolved at the receiver based on different CRC check.

**Table 1.3.1.3.1.1-1. Supported Transmit Formats on Reverse Traffic Channel**

Data Rate [kbps]	Transmit Format	Bandwidth [6.4 kHz]	Duration [frames]	Packet Size	Packet Type	Pilot Pattern	RRI Bits
0	N/A	1 or 2	1	0	NULL	Normal	00
2.4	(1,1,48)	1	1	48	Voice	Normal	01
	(1,4,192)	1	4	192	Data		
4.8	(1,1,96)	1	1	96	Voice	Normal	10
	(1,2,192)	1	2	192	Data		
9.6	(1,1,192)	1	1	192	Voice	Normal	11
	(1,1,192)	1	1	192	Data		
0.64	(1,20,256)	1	20	256	Data	Normal	00
1.28	(1,10,256)	1	10	256	Data	Normal	11
2.4	(2,1,48)	2	1	48	Voice	Normal	01
	(2,4,192)	2	4	192	Data		
4.8	(2,1,96)	2	1	96	Voice	Normal	10

<b>Data Rate [kbps]</b>	<b>Transmit Format</b>	<b>Bandwidth [6.4 kHz]</b>	<b>Duration [frames]</b>	<b>Packet Size</b>	<b>Packet Type</b>	<b>Pilot Pattern</b>	<b>RRI Bits</b>
4.8	(2,2,192)	2	2	192	Data	Normal	10
9.6	(2,1,192)	2	1	192	Voice	Normal	11
	(2,1,192)	2	1	192	Data		
12.8	(2,1,256)	2	1	256	Data	Marked	00
19.2	(2,1,384)	2	1	384	Data	Marked	01
25.6	(2,1,512)	2	1	512	Data	Marked	10
38.4	(2,1,768)	2	1	768	Data	Marked	11

1

**Table 1.3.1.3.1.1-2. Modulation Parameters for the Reverse Traffic Channel**

<b>Transmit Format</b>	<b>Bandwidth [6.4 kHz]</b>	<b>Duration [frames]</b>	<b>Packet Size</b>	<b>Data Rate [kbps]</b>	<b>Code</b>	<b>Rate</b>	<b>Const</b>	<b>Repetition</b>
(1,1,48)	1	1	48	2.4	Conv.	1/4	QPSK	N/A
(1,4,192)	1	4	192	2.4	Conv.	1/4	QPSK	N/A
(1,1,96)	1	1	96	4.8	Conv.	1/2	QPSK	N/A
(1,2,192)	1	2	192	4.8	Conv.	1/2	QPSK	N/A
(1,1,192)	1	1	192	9.6	Conv.	2/3	8PSK	N/A
(1,20,256)	1	20	256	0.64	Turbo	1/5	BPSK	1.5
(1,10,256)	1	10	256	1.28	Turbo	4/15	BPSK	N/A
(2,1,48)	2	1	48	2.4	Conv.	1/4	BPSK	N/A
(2,4,192)	2	4	192	2.4	Conv.	1/4	BPSK	N/A
(2,1,96)	2	1	96	4.8	Conv.	1/4	QPSK	N/A
(2,2,192)	2	2	192	4.8	Conv.	1/4	QPSK	N/A
(2,1,192)	2	1	192	9.6	Conv.	1/2	QPSK	N/A
(2,1,256)	2	1	256	12.8	Turbo	2/3	QPSK	N/A
(2,1,384)	2	1	384	19.2	Turbo	1/2	16-QAM	N/A
(2,1,512)	2	1	512	25.6	Turbo	2/3	16-QAM	N/A
(2,1,768)	2	1	768	38.4	Turbo	2/3	64-QAM	N/A

2

1 For 640 bps and 1.28 kbps data rates, the multi-frame packets shall be encoded over the  
 2 entire physical layer packet. For 2.4 kbps, 4.8 kbps and 9.6 kbps data rates, the multi-  
 3 frame packets shall be encoded separately for each frame (i.e. encoding block size shall  
 4 correspond to single 20 ms frame of data). Rates greater than 9.6 kbps shall always use  
 5 single frame packets.

6 1.3.1.3.1.2 Data Rates

7 The access terminal shall transmit information on the Access Channel at a data rate of 2.4  
 8 kbps. The access terminal shall transmit information on the Reverse Traffic Channel at one  
 9 of the 10 different data rates: 0 (Null rate), 640 bps, 1.28 kbps, 2.4 kbps, 4.8 kbps, 9.6  
 10 kbps, 12.8 kbps, 19.2 kbps, 25.6 kbps and 38.4 kbps.

11 1.3.1.3.2 Access Channel

12 The Access Channel is used by the access terminal to initiate communication with the  
 13 access network or to respond to an access terminal directed message. The Access Channel  
 14 consists of a Pilot Channel and a Data Channel.

15 The Access Channel shall use the same 20 ms frame structure as the Reverse Traffic  
 16 Channel. All the MAC Channel related symbols (namely RRI and CQI) shall be replaced by  
 17 the pilot symbols.

18 The Access Channel shall support (1,4,192) transmit format, namely a 192-bit data packet  
 19 transmitted in 6.4 kHz channel that lasts four 20 ms frames which corresponds to 2.4 kbps  
 20 data rate. Each frame consists of 48 bits and shall be encoded separately using a rate 1/4  
 21 tailbiting convolutional code. The coded bits shall be QPSK modulated. Table 1.3.1.3.2-1  
 22 summarizes the modulation and packet format information for the Access Channel.

23 **Table 1.3.1.3.2-1. Modulation Parameters for the Access Channel**

<b>Data Rate (kbps)</b>	<b>Physical Layer Packets Size (bits)</b>	<b>C R C</b>	<b>T A I L</b>	<b>MAC Packet (bits)</b>	<b>Code</b>	<b>Code Rate</b>	<b>Encod-ing Block Size (bits)</b>	<b>Packet Duratio n (ms)</b>	<b>Mod-ulation Type</b>	<b>BW kHz</b>
2.4	192	16	0	176	Tailbiting Conv	1/4	48	80	QPSK	6.4

24 An access probe shall consist of a preamble followed by one or more Access Channel  
 25 physical layer packets. During the preamble, all the symbols in a frame shall be pilot  
 26 symbols. The preamble length is specified by the parameter PreambleLength in units of  
 27 frames.

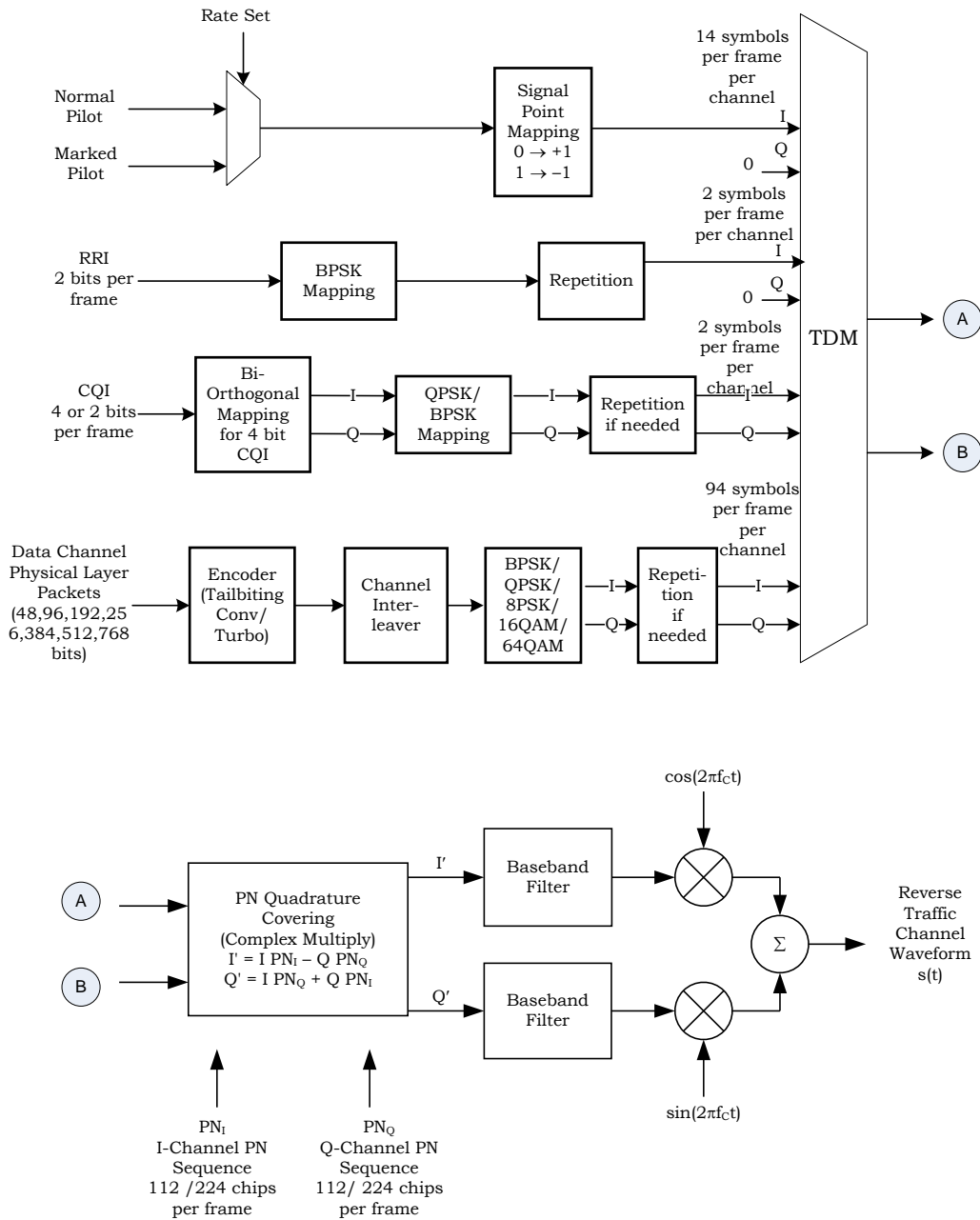
28 1.3.1.3.3 Reverse Traffic Channel

29 The Reverse Traffic Channel is used by the access terminal to transmit user-specific traffic  
 30 or signaling information to the access network. The Reverse Traffic Channel consists of a  
 31 Pilot Channel, a RRI Channel, a CQI Channel, and a Data Channel.

1 The access terminal supports transmission of information on the Data Channel of the  
 2 Reverse Traffic Channel at one of the 10 different data rates: 0 (Null rate), 640 bps, 1.28  
 3 kbps, 2.4 kbps, 4.8 kbps, 9.6 kbps, 12.8 kbps, 19.2 kbps, 25.6 kbps and 38.4 kbps.

4 The structure of the Reverse Traffic Channel is shown in Figure 1.3.1.3.3-1.

5  
 6



**Figure 1.3.1.3.3-1. Reverse Traffic Channel Structure**

1 1.3.1.3.3.1 Pilot Channel

2 Two types of pilot patterns are defined. They are called normal pilot and marked pilot.

3 For 6.4 kHz channel assignment, only the normal pilot consisting of 14 binary ‘0’ shall be  
4 used.

5 For 12.8 kHz channel assignment, both the normal and the marked pilot patterns shall be  
6 used. The two pilot patterns are defined as below.

7 Normal pilot: 28 binary value ‘0’s.

8 Marked pilot: 01010101010101 01010101010101, i.e. alternating binary value of  
9 ‘0’ and ‘1’.

10 The pilot pattern is used to identify data rate set 1 and 2 as defined in 1.3.1.3.3.2.

11 All the pilot symbols shall be BPSK modulated as specified in Table 1.3.1.3.6.1-1.

12 1.3.1.3.3.2 Reverse Rate Indicator Channel

13 Reverse Rate Indicator (RRI) channel shall be used by an access terminal to indicate the  
14 data rate at which a physical layer packet is transmitted on the Reverse Traffic Channel.  
15 The Reverse Traffic Channel supports 10 different data rates, namely 0 (Null rate), 640 bps,  
16 1.28 kbps, 2.4 kbps, 4.8 kbps, 9.6 kbps, 12.8 kbps, 19.2 kbps, 25.6 kbps and 38.4 kbps.  
17 Excluding the Null rate, these data rates are separated into three rate sets, which are  
18 defined in Table 1.3.1.3.3.2-1. For 12.8 kHz channel assignment, the data rates in rate set  
19 1 and 2 shall be supported. Two different pilot patterns, namely normal and marked pilot,  
20 shall be used to differentiate the rate set 1 and 2. A 2-bit RRI field shall be used to indicate  
21 the specific data rate within each rate set. For 6.4 kHz channel assignment, the data rates  
22 in rate set 0 and 1 shall be supported. In this case both rate set 0 and 1 shall use the  
23 same normal pilot pattern.

24 The 2-bit RRI shall be mapped into two BPSK symbols,  $r_{0r1}$ , as shown in Table  
25 1.3.1.3.3.2-1. For 6.4 kHz channel assignment, these two symbols shall be transmitted at  
26 the beginning of a frame, as shown in Figure 1.3.1.3.1-2. For 12.8 kHz channel  
27 assignment, these two BPSK symbols shall be repeated to a four symbol sequence  $r_{0r0r1r1}$ ,  
28 and sent at the beginning of a frame, as shown in Figure 1.3.1.3.1-3.

29 **Table 1.3.1.3.3.2-1. Reverse Traffic Channel Data Rate Table and RRI Mapping**

RRI Bits	BPSK Symbol $r_{0r1}$	Data Rate Set 0 (kbps)	Data Rate Set 1 (kbps)	Data Rate Set 2 (kbps)
00	1, 1	0.64	N/A	12.8
01	1, -1	N/A	2.4	19.2
10	-1, 1	N/A	4.8	25.6
11	-1, -1	1.28	9.6	38.4
Note		Normal pilot 1 bit RRI repeated	Normal Pilot 2 bit RRI	Marked Pilot 2 bit RRI

		Used with 6.4 kHz channel assignment	Used with 6.4 or 12.8 kHz channel assignment	Used with 12.8 kHz channel assignment
--	--	--------------------------------------	--	---------------------------------------

1

2 1.3.1.3.3.3 Channel Quality Indicator Channel

3 Channel Quality Indicator (CQI) Channel shall be used by an access terminal to indicate to  
4 the access network the requested data rate on the Forward Traffic Channel.

5 Two types of CQI formats shall be supported. The first type is the 4-bit CQI format. Using  
6 this CQI format, a terminal can request a data rate from the entire set of Subtype 2 forward  
7 link data rates ranging from 38.4 kbps to 3.072 Mbps. The second type of CQI format uses  
8 two bits for CQI. It is intended for those terminals whose link budget can support only a  
9 subset of forward link data rates and/or whose return link rates are low, i.e., 640 bps or  
10 1.2 kbps. Use of 2-bit CQI format reduces the time required to demodulate the CQI  
11 information for the same level of reliability as that for the 4-bit format. The choice of CQI  
12 format is based on the terminal capability indicated in the RouteUpdate message.

13 1.3.1.3.3.3.1 4-bit CQI format

14 In this format, the requested Forward Traffic Channel data rate is mapped into a 4-bit CQI  
15 value. 4-bit CQI shall be bi-orthogonally encoded into 8 symbols  $b_0 \sim b_7$ , as shown in Table  
16 1.3.1.3.3.3.1-1, and mapped into 4 QPSK symbols as specified below.

17  $C_i = 1+j$  if  $b_{2i}b_{2i+1} = '00'$   
 18  $1-j$  if  $b_{2i}b_{2i+1} = '01'$   
 19  $-1+j$  if  $b_{2i}b_{2i+1} = '10'$   
 20  $-1-j$  if  $b_{2i}b_{2i+1} = '11'$

21 where  $i=0, 1, 2$  or  $3$ . Two out of the four QPSK symbols shall be transmitted in each frame  
22 in order, starting from  $C_0C_1$ . For 6.4 kHz channel assignment, these two symbols shall be  
23 transmitted at the end of a frame, as shown in Figure 1.3.1.3.1-2. For 12.8 kHz channel  
24 assignment, the two symbols  $C_i C_{i+1}$  shall be repeated to a four symbol sequence  $C_i C_i$   
25  $C_{i+1}C_{i+1}$ , which shall be transmitted at the end of a frame, as shown in Figure 1.3.1.3.1-3.  
26 It takes two frames to send all 4 bits of CQI information.

27

**Table 1.3.1.3.3.3.1-1. Bi-orthogonal Mapping of 4 CQI Bits**

4-bit CQI Value	Bi-orthogonal Mapping $b_0b_1b_2b_3 b_4b_5b_6b_7$	FL Data Rate (kbps)
0	0000 0000	0
1	0101 0101	38.4
2	0011 0011	76.8
3	0110 0110	153.6

<b>4-bit CQI Value</b>	<b>Bi-orthogonal Mapping</b> <b>b<sub>0</sub>b<sub>1</sub>b<sub>2</sub>b<sub>3</sub> b<sub>4</sub>b<sub>5</sub>b<sub>6</sub>b<sub>7</sub></b>	<b>FL Data Rate (kbps)</b>
4	0000 1111	307.2
5	0101 1010	307.2
6	0011 1100	614.4
7	0110 1001	614.4
8	1111 1111	921.6
9	1010 1010	1228.8
10	1100 1100	1228.8
11	1001 1001	1843.2
12	1111 0000	2457.6
13	1010 0101	1536
14	1100 0011	3072
15	1001 0110	Reserved

1 1.3.1.3.3.3.2 2-bit CQI format

2 In this format, only a subset of Forward Traffic Channel data rates can be requested using  
3 2-bit CQI. The 2-bit CQI and the corresponding forward link data rate are listed in Table  
4 1.3.1.3.3.3.2-1. Each CQI bit shall be mapped to a BPSK symbol. For 6.4 kHz channel  
5 assignment, these two CQI symbols shall be transmitted at the end of a frame, as shown in  
6 Figure 1.3.1.3.1-2. For 12.8 kHz channel assignment, the two symbols  $C_i$   $C_{i+1}$  shall be  
7 repeated to a four symbol sequence,  $C_i$   $C_i$   $C_{i+1}$   $C_{i+1}$  and sent at the end of a frame, as shown  
8 in Figure 1.3.1.3.1-3. It takes one frame to send all 2 bits of CQI information.

9 **Table 1.3.1.3.3.3.2-1. Mapping of 2 CQI Bits**

<b>2 bit CQI Value</b>	<b>BPSK Mapping</b> <b>b<sub>0</sub>b<sub>1</sub></b>	<b>FL Data Rate Metric (kbps)</b>
0	00	38.4
1	01	76.8
2	10	153.6
3	11	307.2

10

11 1.3.1.3.3.3.3 CQI Channel Operation

12 The parameter CQIPeriod specifies a time period called CQI period in units of frames.  
13 During a reverse link CQI period, the access terminal shall transmit a single CQI value.

1 During a forward link CQI period, the access network transmits to the access terminal at  
 2 the single requested data rate. The forward link CQI period and reverse link CQI period  
 3 have the same duration defined by CQIPeriod, but their starting times are staggered by a  
 4 fixed delay defined as CQIDelay, as illustrated in Figure 1.3.1.3.3.3-1.

5 The forward link data rate to an access terminal shall be changed only at the start of each  
 6 forward link CQI period as specified by the following equation:

7 
$$(T - \text{FrameOffset}) \bmod (\text{CQIPeriod} * 12 \text{ slots/frame}) = 0$$

8 where T is the CDMA system time and FrameOffset is the traffic channel frame offset  
 9 specified in TrafficChannelAssignment message, both of which are in units of slots.

10 The parameter CQIDelay specifies the delay in units of frames between the start time of the  
 11 reverse link CQI period and the corresponding start time of the forward link CQI period at  
 12 the access terminal. It defines the delay from the time an access terminal starts to send a  
 13 new CQI value in a new reverse link CQI period until the terminal begins to receive the  
 14 requested forward link data rate as determined by the CQI value in a new forward link CQI  
 15 period, as illustrated in Figure 1.3.1.3.3.3-1. It is required that

16 
$$\text{CQIDelay} = \text{CQIPeriod} + \text{MaxPathDelay}$$

17 where MaxPathDelay ≥ maximum round trip delay plus access network processing delay.

18 An access terminal shall start a new reverse link CQI period by sending a new CQI value at  
 19 its local CDMA time, T<sub>AT</sub>, which satisfies

20 
$$(T_{AT} - \text{FrameOffset} - \text{CQIDelay in slots}) \bmod (\text{CQIPeriod} * 12 \text{ slots/frame}) = 0$$

21 Table 1.3.1.3.3.3-1 summarizes the timing alignment for the CQI channel operation. T<sub>AT</sub>  
 22 and T<sub>AN</sub> denote the CDMA system time observed at access terminal and access network,  
 23 respectively, for the nth forward link CQI period. T<sub>AT</sub> lags behind T<sub>AN</sub> by half of the actual  
 24 roundtrip path delay.

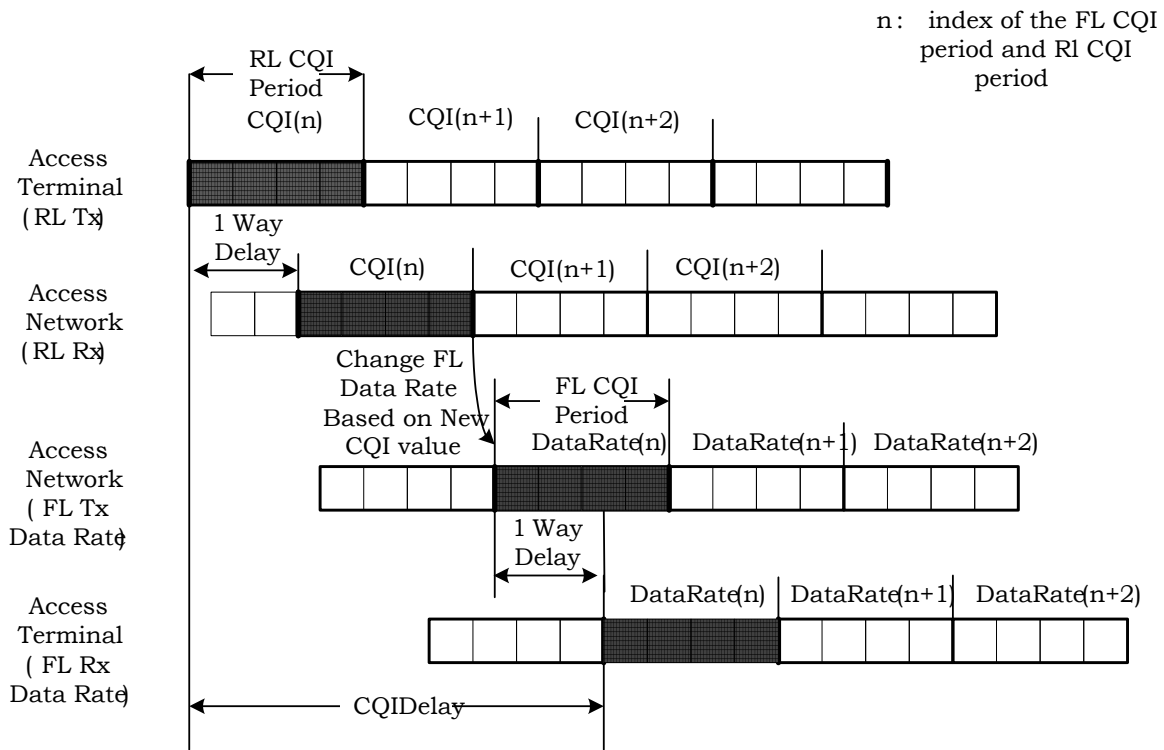
25 **Table 1.3.1.3.3.3-1. CQI Channel Timing Alignment**

Local CDMA Time	Start of the nth CQI Period	End of the nth CQI Period
AT Reverse Transmits New CQI Value	T <sub>AT</sub> - CQIDelay	T <sub>AT</sub> - CQIDelay + CQIPeriod
AN Reverse Receives New CQI Value	T <sub>AN</sub> - CQIPeriod - (MaxPathDelay - ActualPathDelay)	T <sub>AN</sub> - (MaxPathDelay - ActualPathDelay)
AN Forward Transmits New Data Rate	T <sub>AN</sub>	T <sub>AN</sub> + CQIPeriod
AT Forward Receives New Data Rate	T <sub>AT</sub>	T <sub>AT</sub> + CQIPeriod

26 During the call setup, the access terminal shall send the initial CQI value in RouteUpdate  
 27 message. Both the access terminal and the access network shall use this initial CQI value

1 until the access network receives a new CQI value from the terminal and starts the first  
 2 CQI period.

3



4

**Figure 1.3.1.3.3.3-1. CQI Channel Timing Illustration**

(Not drawn to scale)

5

6

7 1.3.1.3.3.4 Data Channel

8 The Data Channel is used by an access terminal to transmit physical layer packets at data  
 9 rates given in Table 1.3.1.3.1.1-2.

10 1.3.1.3.4 Encoding

11 Two types of encoding are used for the Reverse Traffic Channel. A physical layer packet of  
 12 size less than or equal to 192 bits shall be encoded using a constraint length 11  
 13 convolutional code. A physical layer packet of size larger than 192 bits shall be encoded  
 14 using a Turbo Code. The code rate is determined by the data rate and the bandwidth  
 15 assigned.

16 1.3.1.3.4.1 Convolutional Encoding

17 Convolutional encoding shall be used for packets of size 48, 96 or 192 bits. A physical layer  
 18 packet shall be divided into one or multiple encoding blocks, each of which spans one 20  
 19 msec frame duration. Each encoding block shall be independently encoded. For an  
 20 encoding block of size 48 or 96 bits, tailbiting convolutional encoding shall be used. For an  
 21 encoding block of size 192 bits, convolutional encoding with 10 bits of zero tail shall be

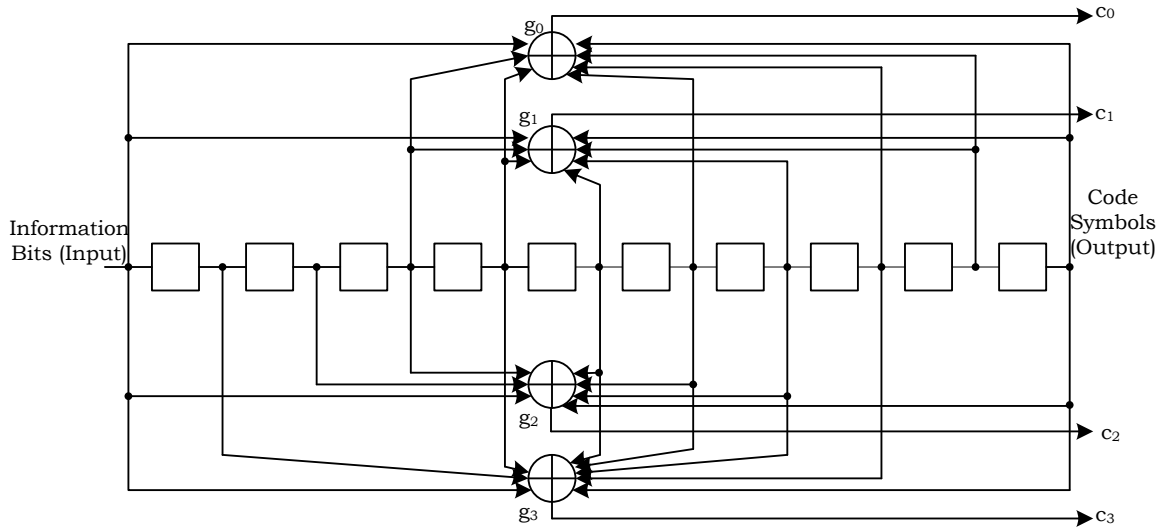
1 used. The Reverse Traffic Channel supports three convolutional code rates, namely 1/4,  
 2 1/2 and 2/3. Table 1.3.1.3.4.1-1 provides the code rate and other convolution encoding  
 3 related information.

4 **Table 1.3.1.3.4.1-1. Convolution Code Rate Table**

<b>BW [6.4 kHz]</b>	<b>Data Rate [kbps]</b>	<b>Packet Type</b>	<b>Packet Size [bits]</b>	<b>Encoding Block Size [bits]</b>	<b># of Encoding Block</b>	<b>Code</b>	<b>Rate</b>	<b>Modulation</b>
1	2.4	Voice	48	48	1	Tailbiting	1/4	QPSK
		Data	192	48	4	Conv.		
1	4.8	Voice	96	96	1	Tailbiting	1/2	QPSK
		Data	192	96	2	Conv.		
1	9.6	Voice	192	192	1	Regular	2/3	8PSK
		Data	192	192	1	Conv.		
2	2.4	Voice	48	48	1	Tailbiting	1/4	BPSK
		Data	192	48	4	Conv.		
2	4.8	Voice	96	96	1	Tailbiting	1/4	QPSK
		Data	192	96	2	Conv.		
2	9.6	Voice	192	192	1	Regular	1/2	QPSK
		Data	192	192	1	Conv.		

5  
 6 The generator functions for the rate 1/4 constraint length 11 code shall be  $g_0$  equals 4656  
 7 (octal),  $g_1$  equals 4726 (octal),  $g_2$  equals 5562 (octal), and  $g_3$  equals 6372 (octal). This code  
 8 generates four code symbols for each data bit input to the encoder. These code symbols  
 9 shall be output so that the code symbol ( $c_0$ ) encoded with generator function  $g_0$  is output  
 10 first, the code symbol ( $c_1$ ) encoded with generator function  $g_1$  is output second, the code  
 11 symbol ( $c_2$ ) encoded with generator function  $g_2$  is output third, and the code symbol ( $c_3$ )  
 12 encoded with generator function  $g_3$  is output last. The first code symbol that is output after  
 13 initialization shall be a code symbol encoded with generator function  $g_0$ . The encoder for  
 14 this code is illustrated in Figure 1.3.1.3.4.1-1.

15



**Figure 1.3.1.3.4.1-1. K = 11, Rate 1/4 Convolutional Encoder**

For regular convolutional encoding with 10 bits of zero tail, all the encoder shift registers shall be initialized to '0's. For the tailbiting encoding, the encoder shift-registers shall be initialized with the last 10 bits of an encoding block.

The rate 1/2 convolutional code shall be obtained by puncturing the rate 1/4 code by using only the first and fourth generator polynomials  $g_0$  and  $g_3$ .

The rate 2/3 convolutional code shall be generated by puncturing the rate 1/2 convolutional code as specified in Table 1.3.1.3.4.1-2. Within a puncturing pattern, a '0' means that the symbol shall be deleted and a '1' means that the symbol shall be passed onwards.

**Table 1.3.1.3.4.1-2. Puncturing Pattern for Rate 2/3 Convolutional Code**

Output	Rate 2/3 Puncture Pattern
$c_0$	1011
$c_3$	1110

Note: The puncturing table shall be read first from top to bottom and then from left to right.

1.3.1.3.4.2 Turbo Encoding

A physical layer packet with size larger than 192 bits shall be encoded using a Turbo Code. In this case the encoding block is the entire physical layer packet. The choice of code rate is dependent on data rate and number of channel assigned as shown in Table 1.3.1.3.4.2-1.

1

**Table 1.3.1.3.4.2-1. Turbo Code Rate Table**

<b>BW [6.4 kHz]</b>	<b>Data Rate [kbps]</b>	<b>Packet Size [bits]</b>	<b>Code</b>	<b>Rate</b>	<b>Modulation</b>
1	0.64	256	Turbo	1/5	BPSK
1	1.28	256	Turbo	4/15	BPSK
2	12.8	256	Turbo	2/3	QPSK
2	19.2	384	Turbo	1/2	16-QAM
2	25.6	512	Turbo	2/3	16-QAM
2	38.4	768	Turbo	2/3	64-QAM

2 The turbo encoder encodes the input data and adds an output tail sequence. If the total  
3 number of input bits is  $N_{\text{turbo}}$ , the turbo encoder generates  $N_{\text{turbo}}/R$  encoded data output  
4 symbols followed by  $6/R$  tail output symbols, where  $R$  is the code rate of  $1/3$  or  $1/5$ . The  
5 turbo encoder employs two systematic, recursive, convolutional encoders connected in  
6 parallel, with an interleaver, the turbo interleaver, preceding the second recursive  
7 convolutional encoder.

8 The two recursive convolutional codes are called the constituent codes of the turbo code.  
9 The outputs of the constituent encoders are punctured and repeated to achieve the  $(N_{\text{turbo}}$   
10  $+ 6)/R$  output symbols.

#### 11 1.3.1.3.4.2.1 Turbo Encoders

12 The turbo encoder employs two systematic, recursive, convolutional encoders connected in  
13 parallel, with an interleaver, the turbo interleaver, preceding the second recursive  
14 convolutional encoder. The two recursive convolutional codes are called the constituent  
15 codes of the turbo code. The outputs of the constituent encoders are punctured and  
16 repeated to achieve the desired number of turbo encoder output symbols.

17 A common constituent code shall be used for the rate  $1/3$ , and  $1/5$  Turbo codes. The  
18 transfer function for the constituent code shall be

$$19 \quad G(D) = \begin{bmatrix} 1 & \frac{n_0(D)}{d(D)} & \frac{n_1(D)}{d(D)} \end{bmatrix}$$

20 where  $d(D) = 1 + D^2 + D^3$ ,  $n_0(D) = 1 + D + D^3$ , and  $n_1(D) = 1 + D + D^2 + D^3$ .

21 The turbo encoder shall generate an output symbol sequence that is identical to the one  
22 generated by the encoder shown in Figure 1.3.1.3.4.2.2-1. Initially, the states of the  
23 constituent encoder registers in this figure are set to zero. Then, the constituent encoders  
24 are clocked with the switches in the positions noted.

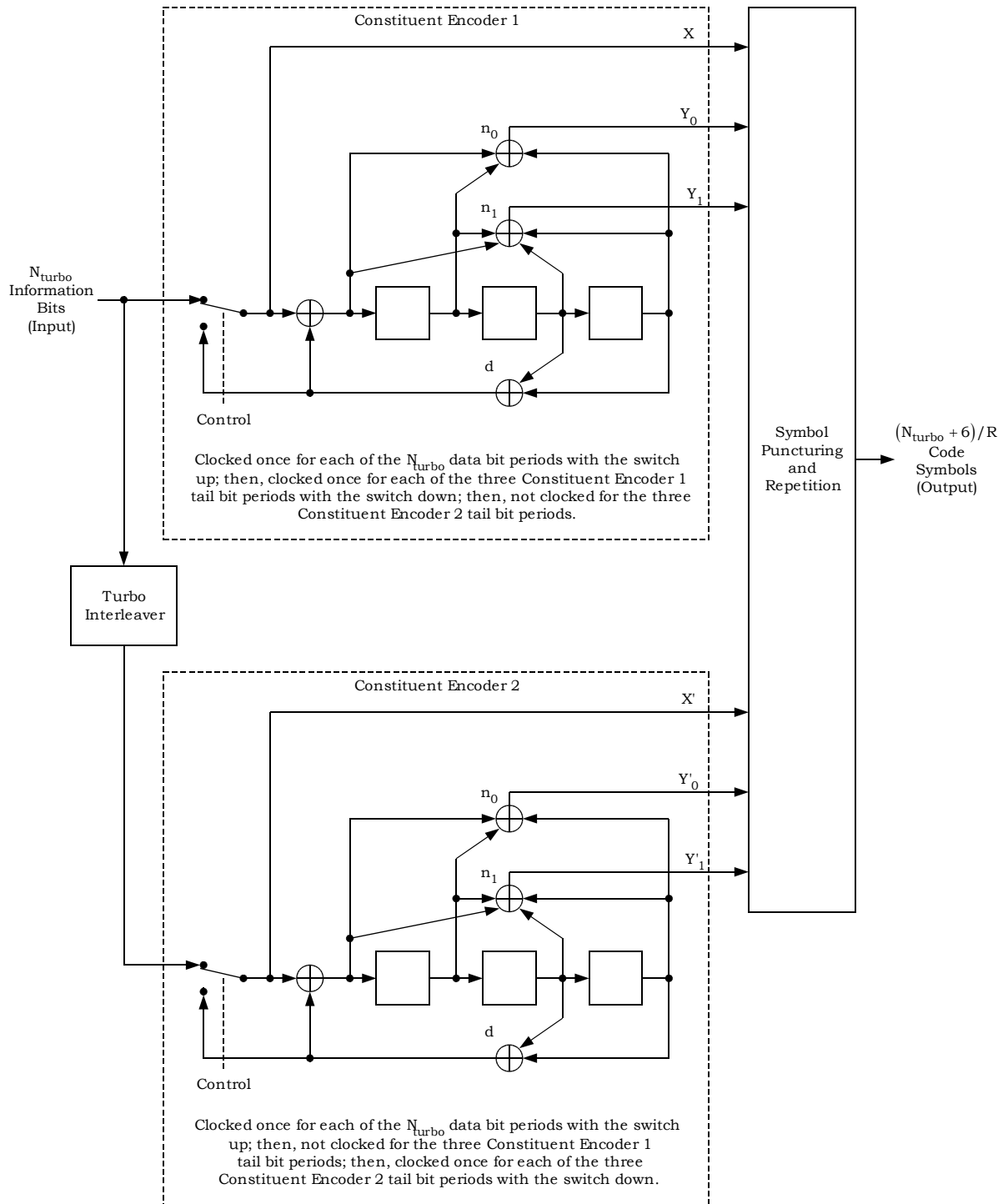
25 The encoded data output symbols are generated by clocking the constituent encoders  
26  $N_{\text{turbo}}$  times with the switches in the up positions and puncturing the outputs as specified  
27 in Table 1.3.1.3.4.2.2-1. Within a puncturing pattern, a '0' means that the symbol shall be  
28 deleted and a '1' means that the symbol shall be passed onwards. The constituent encoder

1 outputs for each bit period shall be output in the sequence  $X, Y_0, Y_1, X', Y'_0, Y'_1$  with the  $X$   
2 output first. Symbol repetition is not used in generating the encoded data output symbols.

### 3 1.3.1.3.4.2.2 Turbo Code Termination

4 The turbo encoder shall generate  $6/R$  tail output symbols following the encoded data  
5 output symbols. This tail output symbol sequence shall be identical to the one generated by  
6 the encoder shown in Figure 1.3.1.3.4.2.2-1. The tail output symbols are generated after  
7 the constituent encoders have been clocked  $N_{\text{turbo}}$  times with the switches in the up  
8 position. The first  $3/R$  tail output symbols are generated by clocking Constituent Encoder 1  
9 three times with its switch in the down position while Constituent Encoder 2 is not clocked  
10 and puncturing and repeating the resulting constituent encoder output symbols. The last  
11  $3/R$  tail output symbols are generated by clocking Constituent Encoder 2 three times with  
12 its switch in the down position while Constituent Encoder 1 is not clocked and puncturing  
13 and repeating the resulting constituent encoder output symbols. The constituent encoder  
14 outputs for each bit period shall be output in the sequence  $X, Y_0, Y_1, X', Y'_0, Y'_1$  with the  $X$   
15 output first.

16 The constituent encoder output symbol puncturing and symbol repetition shall be as  
17 specified in Table 1.3.1.3.4.2.2-2. Within a puncturing pattern, a '0' means that the symbol  
18 shall be deleted and a '1' means that the symbol shall be passed onwards. For rate  $1/5$   
19 turbo codes, the tail output code symbols for each of the first three tail bit periods shall be  
20 punctured and repeated to achieve the sequence  $XXY_0Y_1Y_1$ , and the tail output code  
21 symbols for each of the last three tail bit periods shall be punctured and repeated to  
22 achieve the sequence  $X'X'Y'_0Y'_1Y'_1$ . For rate  $1/3$  turbo codes, the tail output symbols for  
23 each of the first three tail bit periods shall be  $XXY_0$ , and the tail output symbols for each of  
24 the last three tail bit periods shall be  $X'X'Y'_0$ .



**Figure 1.3.1.3.4.2.2-1. Turbo Encoder**

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2

1

**Table 1.3.1.3.4.2.2-1. Puncturing Patterns for the Data Bit Periods**

Output	Code Rate	
	1/3	1/5
X	1	1
Y <sub>0</sub>	1	1
Y <sub>1</sub>	0	1
X'	0	0
Y' <sub>0</sub>	1	1
Y' <sub>1</sub>	0	1

Note: For each rate, the puncturing table shall be read first from top to bottom and then from left to right.

2

3

**Table 1.3.1.3.4.2.2-2. Puncturing Patterns for the Tail Bit Periods**

Output	Code Rate	
	1/3	1/5
X	111 000	111 000
Y <sub>0</sub>	111 000	111 000
Y <sub>1</sub>	000 000	111 000
X'	000 111	000 111
Y' <sub>0</sub>	000 111	000 111
Y' <sub>1</sub>	000 000	000 111

Note: For rate 1/3 turbo codes, the puncturing table shall be read first from top to bottom repeating X and X', and then from left to right. For rate 1/5 turbo codes, the puncturing table shall be read first from top to bottom repeating X, X', Y<sub>1</sub>, and Y'<sub>1</sub> and then from left to right.

4

#### 5 1.3.1.3.4.2.3 Turbo Interleavers

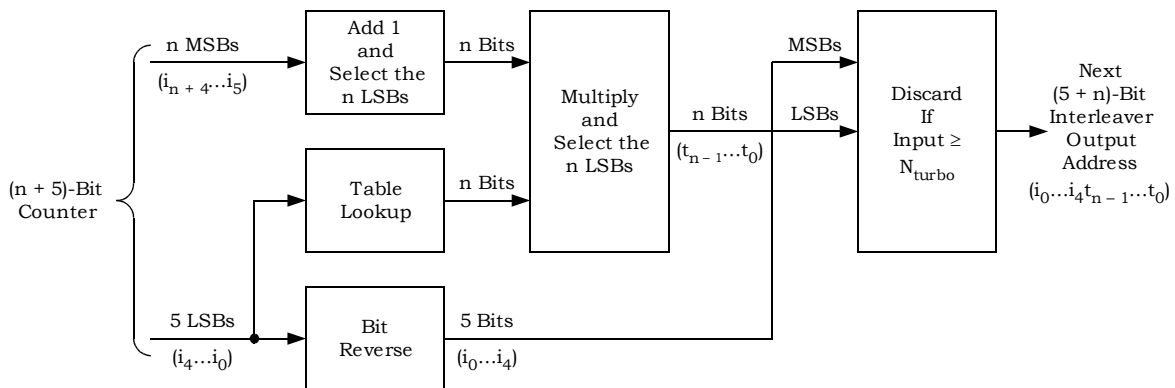
6 The turbo interleaver, which is part of the turbo encoder, shall block interleave the turbo  
7 encoder input data that is fed to Constituent Encoder 2.

8 The turbo interleaver shall be functionally equivalent to an approach where the entire  
9 sequence of turbo interleaver input bits are written sequentially into an array at a sequence

of addresses, and then the entire sequence is read out from a sequence of addresses that are defined by the procedure described below.

Let the sequence of input addresses be from 0 to  $N_{\text{turbo}} - 1$ . Then, the sequence of interleaver output addresses shall be equivalent to those generated by the procedure illustrated in Figure 1.3.1.3.4.2.3-1 and described below.<sup>3</sup>

1. Determine the turbo interleaver parameter,  $n$ , where  $n$  is the smallest integer such that  $N_{\text{turbo}} \leq 2^{n+5}$ . Table 1.3.1.3.4.2.3-1 gives this parameter for the different physical layer packet sizes.
2. Initialize an  $(n + 5)$ -bit counter to 0.
3. Extract the  $n$  most significant bits (MSBs) from the counter and add one to form a new value. Then, discard all except the  $n$  least significant bits (LSBs) of this value.
4. Obtain the  $n$ -bit output of the table lookup defined in Table 1.3.1.3.4.2.3-2 with a read address equal to the five LSBs of the counter. Note that this table depends on the value of  $n$ .
5. Multiply the values obtained in Steps 3 and 4, and discard all except the  $n$  LSBs.
6. Bit-reverse the five LSBs of the counter.
7. Form a tentative output address that has its MSBs equal to the value obtained in Step 6 and its LSBs equal to the value obtained in Step 5.
8. Accept the tentative output address as an output address if it is less than  $N_{\text{turbo}}$ ; otherwise, discard it.
9. Increment the counter and repeat Steps 3 through 8 until all  $N_{\text{turbo}}$  interleaver output addresses are obtained.



**Figure 1.3.1.3.4.2.3-1. Turbo Interleaver Output Address Calculation Procedure**

<sup>3</sup> This procedure is equivalent to one where the counter values are written into a  $2^5$ -row by  $2^n$ -column array by rows, the rows are shuffled according to a bit-reversal rule, the elements within each row are permuted according to a row-specific linear congruential sequence, and tentative output addresses are read out by column. The linear congruential sequence rule is  $x(i + 1) = (x(i) + c) \text{ mod } 2^n$ , where  $x(0) = c$  and  $c$  is a row-specific value from a table lookup.

1

**Table 1.3.1.3.4.2.3-1. Turbo Interleaver Parameter**

<b>Physical Layer Packet Size</b>	<b>Turbo Interleaver Block Size <math>N_{\text{turbo}}</math></b>	<b>Turbo Interleaver Parameter <b>n</b></b>
256	250	3
384	378	4
512	506	4
768	762	5

2

1

**Table 1.3.1.3.4.2.3-2. Turbo Interleaver Lookup Table Definition**

<b>Table Index</b>	<b>n = 3 Entries</b>	<b>n = 4 Entries</b>	<b>n = 5 Entries</b>
0	1	5	27
1	1	15	3
2	3	5	1
3	5	15	15
4	1	1	13
5	5	9	17
6	1	9	23
7	5	15	13
8	3	13	9
9	5	15	3
10	3	7	15
11	5	11	3
12	3	15	13
13	5	3	1
14	5	15	13
15	1	5	29
16	3	13	21
17	5	15	19
18	3	9	1
19	5	3	3
20	3	1	29
21	5	3	17
22	5	15	25
23	5	1	29
24	1	13	9
25	5	1	13
26	1	9	23
27	5	15	13
28	3	11	13
29	5	3	1
30	5	15	13
31	3	5	13

2 The code rates of  $2/15$  and  $4/15$  shall be obtained by puncturing and/or repetition of the  
3 base rate  $1/5$  code, and the code rates of  $1/2$  and  $2/3$  shall be obtained by puncturing of  
4 the base rate  $1/3$  code. Refer to 1.3.1.3.5 for details on the interleaving and puncturing.

1

## 2 1.3.1.3.5 Channel Interleaving

3 The sequence of binary symbols at the output of the encoder shall be interleaved with a  
4 channel interleaver.

## 5 1.3.1.3.5.1 Channel Interleaver for Convolutional Code

6 There are three different channel interleavers for convolutional encoder outputs  
7 corresponding to three different encoder output block sizes.

## 8 1.3.1.3.5.1.1 192-symbol Channel Interleaver

9 This interleaver shall be used for 6.4 kHz channel 2.4 kbps, 6.4 kHz channel 4.8 kbps and  
10 12.8 kHz channel 2.4 kbps data rates. The interleaving is based on 2-D matrix  
11 interleaving. The Matrix Interleaving operation is carried out in the following steps:

- 12 1. 192 encoded symbols are written into a two dimensional matrix with  $R=3$  rows and  
13  $C=64$  columns with row-index incrementing first, followed by column-index. The  $i^{\text{th}}$   
14 input symbol,  $0 \leq i < 192$ , goes into  $r^{\text{th}}$  row= $\text{mod}(i,R)$  and  $c^{\text{th}}$  column= $\text{floor}(i/R)$ .
- 15 2. The linear array of  $C$  symbols, at each given row, is bit-reverse interleaved based on  
16 its column-index.
- 17 3. Symbols from the 2-D matrix are read out with column-index incrementing first,  
18 followed by row-index. In other words, the  $i^{\text{th}}$  output symbol ( $r \times C + c$ ), where  $0 \leq i$   
19  $< 192$  comes from the  $r^{\text{th}}$  row,  $c^{\text{th}}$  column, where  $0 \leq r < 3$  and  $0 \leq c < 64$ .

## 20 1.3.1.3.5.1.2 288-symbol Channel Interleaver

21 This interleaver shall be used for 6.4 kHz channel 9.6 kbps data rate. The interleaving shall  
22 consist of a Symbol Grouping and Reordering stage followed by a Matrix Interleaving stage.

## 23 1.3.1.3.5.1.2.1 Symbol Grouping and Reordering

24 For rate  $2/3$  convolutional encoder output symbol sequence, the position of  $i^{\text{th}}$  and  $(i+1)^{\text{th}}$   
25 symbol shall be swapped, where  $0 \leq i < 288$  and  $\text{mod}(i,6)=3$ .

## 26 1.3.1.3.5.1.2.2 Matrix Interleaving

27 The Matrix Interleaving operation is carried out in the following steps:

- 28 1. 288 re-ordered symbols are written into a 3-dimensional cuboidal array with  $R=3$   
29 rows,  $C=32$  columns, and  $K=3$  levels. Symbols are written into the 3-dimensional  
30 array with level-index incrementing first, followed by row-index, followed by column-  
31 index. In other words, the  $i^{\text{th}}$  incoming symbol  $((c \times R + r) \times K + k)$ , where  $0 \leq i < 288$   
32 goes into the  $r^{\text{th}}$  row,  $c^{\text{th}}$  column, and  $k^{\text{th}}$  level where,  $0 \leq r < 3$ ,  $0 \leq c < 32$ , and  $0 \leq$   
33  $k < 3$ .
- 34 2. The linear array of  $C$  symbols, at each given level and row, is bit-reverse interleaved  
35 based on column-index.

- 1           3. Symbols from the cuboidal array are read out with level-index incrementing first,  
2           followed by column-index, followed by row-index. In other words, the  $i^{\text{th}}$  output  
3           symbol  $((r \times C + c) \times K + k)$ , where  $0 \leq i < 288$  comes from the  $r^{\text{th}}$  row,  $c^{\text{th}}$  column,  
4           and  $k^{\text{th}}$  level, where  $0 \leq r < 3$ ,  $0 \leq c < 32$ , and  $0 \leq k < 3$ .

#### 5   1.3.1.3.5.1.3 384-symbol Channel Interleaver

6   This interleaver shall be used for 12.8 kHz channel 4.8 kbps and 9.6 kbps data rates. The  
7   interleaving is based on 3-D matrix interleaving. The Matrix interleaving operation is  
8   carried out in the following steps:

- 9           1. 384 symbols from the encoder output are written into a 3-dimensional cuboidal  
10           array with  $R=3$  rows,  $C=64$  columns, and  $K=2$  levels. Symbols are written into the  
11           3-dimensional array with level-index incrementing first, followed by row-index,  
12           followed by column-index. In other words, the  $i^{\text{th}}$  incoming symbol  $((c \times R + r) \times K +$   
13            $k)$ , where  $0 \leq i < 384$  goes into the  $r^{\text{th}}$  row,  $c^{\text{th}}$  column, and  $k^{\text{th}}$  level where,  $0 \leq r <$   
14            $3$ ,  $0 \leq c < 64$ , and  $0 \leq k < 2$ .
- 15           2. The linear array of  $C$  symbols, at each given level and row, is bit-reverse interleaved  
16           based on column-index.
- 17           3. Symbols from the cuboidal array are read out with level-index incrementing first,  
18           followed by column-index, followed by row-index. In other words, the  $i^{\text{th}}$  output  
19           symbol  $((r \times C + c) \times K + k)$ , where  $0 \leq i < 288$  comes from the  $r^{\text{th}}$  row,  $c^{\text{th}}$  column,  
20           and  $k^{\text{th}}$  level, where  $0 \leq r < 3$ ,  $0 \leq c < 32$ , and  $0 \leq k < 3$ .

#### 21   1.3.1.3.5.2 Channel Interleaver for Turbo Code

22   Channel interleaving for turbo code shall consist of a Symbol Reordering stage followed by a  
23   Matrix Interleaving stage.

24   The packet length,  $N$  (including data and tail bits) is expressed as  $N = R \times K \times 2^m$ , where,  $R$ ,  
25    $K$  and  $m$  are positive integers. The channel interleaver is described in terms of the  
26   parameters  $R$ ,  $K$ ,  $m$ , and an end-around-shift parameter  $D$ .

##### 27   1.3.1.3.5.2.1 Symbol Reordering

28   Turbo encoder data and tail output symbols generated with the rate-1/5 encoder shall be  
29   reordered according to the following steps:

- 30           1. All of the data and tail turbo encoder output symbols shall be demultiplexed into  
31           five sequences denoted  $U$ ,  $V_0$ ,  $V_1$ ,  $V'_0$ , and  $V'_1$ . The scrambled encoder output  
32           symbols shall be sequentially distributed from the  $U$  sequence to the  $V'_1$  sequence  
33           with the first scrambled encoder output symbol going to the  $U$  sequence, the second  
34           to the  $V_0$  sequence, the third to the  $V_1$  sequence, the fourth to the  $V'_0$  sequence, the  
35           fifth to the  $V'_1$  sequence, the sixth to the  $U$  sequence, etc.
- 36           2. The  $U$ ,  $V_0$ ,  $V_1$ ,  $V'_0$ , and  $V'_1$  sequences shall be ordered according to  $UV_0V'_0V_1V'_1$ .  
37           That is, the  $U$  sequence of symbols shall be first and the  $V'_1$  sequence of symbols  
38           shall be last.

1 The scrambled turbo encoder data and tail output symbols generated with the rate-1/3  
2 encoder shall be reordered according to the following procedure:

- 3 1. All of the scrambled data and tail turbo encoder output symbols shall be  
4 demultiplexed into three sequences denoted  $U$ ,  $V_0$  and  $V'_0$ . The scrambled encoder  
5 output symbols shall be sequentially distributed from the  $U$  sequence to the  $V'_0$   
6 sequence with the first scrambled encoder output symbol going to the  $U$  sequence,  
7 the second to the  $V_0$  sequence, the third to the  $V'_0$  sequence, the fourth to the  $U$   
8 sequence, etc.
- 9 2. The  $U$ ,  $V_0$  and  $V'_0$  sequences shall be ordered according to  $U V_0 V'_0$ . That is, the  $U$   
10 sequence of symbols shall be first and the  $V'_0$  sequence of symbols shall be last.

#### 11 1.3.1.3.5.2.2 Matrix Interleaving

12 The Matrix Interleaving operation is carried out in the following steps:

- 13 1. The  $N$  symbols of the  $U$ -sequence symbols are written into a 3-dimensional cuboidal  
14 array with  $R$  rows,  $C$  columns, and  $K$  levels. Symbols are written into the 3-  
15 dimensional array with level-index incrementing first, followed by column-index,  
16 followed by row-index. In other words, the  $i^{\text{th}}$  incoming symbol  $((r \times C + c) \times K + k)$ ,  
17 where  $0 \leq i < N$  goes into the  $r^{\text{th}}$  row,  $c^{\text{th}}$  column, and  $k^{\text{th}}$  level where,  $0 \leq r < R$ ,  $0 \leq$   
18  $c < C$ , and  $0 \leq k < K$ .
- 19 2. The linear array of  $R$  symbols, at the  $c^{\text{th}}$  column and  $k^{\text{th}}$  level, is end-around-shifted  
20 by  $(c \times K + k) \bmod R$ . In other words,  $\text{matrix}[r][c][k]$  is transformed to  $\text{matrix}[(r + c \times$   
21  $K + k) \bmod R][c][k]$ .
- 22 3. The linear array of  $C$  symbols, at each given level and row, is bit-reverse interleaved  
23 (based on column-index)<sup>4</sup>. Symbols from the cuboidal array are read out with row-  
24 index incrementing first, followed by column-index, followed by level-index. In other  
25 words, the  $i^{\text{th}}$  output symbol  $((k \times C + c) \times R + r)$ , where  $0 \leq i < N$  comes from the  $r^{\text{th}}$   
26 row,  $c^{\text{th}}$  column, and  $k^{\text{th}}$  level, where  $0 \leq r < R$ ,  $0 \leq c < C$ , and  $0 \leq k < K$ .
- 27 4. The  $N$  symbols of the  $V_0$  sequence, followed by the  $N$  symbols of the  $V'_0$  sequence  
28 are written into a 3-dimensional cuboidal array with  $R$  rows,  $C$  columns and  $K$   
29 levels. Symbols are written into the 3-dimensional array with level-index  
30 incrementing first, followed by column-index, followed by row-index. In other words,  
31 the  $i^{\text{th}}$  incoming symbol  $((r \times C + c) \times K + k)$ , where  $0 \leq i < 2 \times N$  goes into the  $r^{\text{th}}$   
32 row,  $c^{\text{th}}$  column, and  $k^{\text{th}}$  level, where  $0 \leq r < R$ ,  $0 \leq c < C$ , and  $0 \leq k < K$ .
- 33 5. The linear array of  $R$  symbols, at the  $c^{\text{th}}$  column and  $k^{\text{th}}$  level, is end-around-shifted  
34 by the amount  $\lfloor (K \times c + k) / D \rfloor \bmod R$ . In other words,  $\text{matrix}[r][c][k]$  is transformed  
35 to  $\text{matrix}[r + \lfloor (K \times c + k) / D \rfloor \bmod R][c][k]$ .

---

<sup>4</sup> If the number of columns  $C$  is not a power of 2, no bit-reverse operation is performed .

- 1 6. The linear array of  $C$  symbols, at each given level and row, is bit-reverse interleaved  
 2 <sup>5</sup> (based on the column-index).
- 3 7. Symbols from the cuboidal array are read out with row-index incrementing first,  
 4 followed by column-index, followed by level-index. In other words, the  $i^{\text{th}}$  output  
 5 symbol  $((k \times C + c) \times R + r)$ , where  $0 \leq i < 2 \times N$  comes from the  $r^{\text{th}}$  row,  $c^{\text{th}}$  column,  
 6 and  $k^{\text{th}}$  level, where,  $0 \leq r < R$ ,  $0 \leq c < C$ , and  $0 \leq k < K$ .
- 7 8. The sequence of  $V_1$  and  $V_1'$  symbols are processed similar to the  $V_0$  and  $V_0'$   
 8 symbols, as described in 4 through 7.

9 Table 1.3.1.3.5.2.2-1 below shows the interleaver parameters for various packets used on  
 10 the Reverse Traffic Channel.

11 **Table 1.3.1.3.5.2.2-1. Channel Interleaver Parameters**

<b>Payload size (bits)</b>	<b>N</b>	<b>K</b>	<b>R</b>	<b>C</b>	<b>D</b>
256	256	1	2	128	1
384	384	1	4	96	1
512	512	1	4	128	1
768	768	1	6	128	1

12

### 13 1.3.1.3.6 Modulation

14 The output of the channel interleaver shall be applied to a modulator that outputs an in-  
 15 phase stream and a quadrature stream of modulated values. The modulator generates  
 16 BPSK, QPSK, 8-PSK, 16-QAM or 64-QAM modulation symbols, depending on the data rate.

#### 17 1.3.1.3.6.1 BPSK Modulation

18 For physical layer packets using BPSK modulation, each channel interleaver output symbol  
 19 shall form a BPSK modulation symbol as specified in Table 1.3.1.3.6.1-1.

20 **Table 1.3.1.3.6.1-1. BPSK Modulation Table**

<b>Interleaved Symbols</b>	<b>Modulation Symbols</b>
0	+D
1	-D

Note:  $D = 1$ .

21

---

<sup>5</sup> If the number of columns  $C$  is not a power of 2, the following pseudo bit inverse operation is performed. For the input column index  $c$ , the output column index shall be  $\text{floor}(c/2) + C/2 * \text{mod}(c,2)$ .

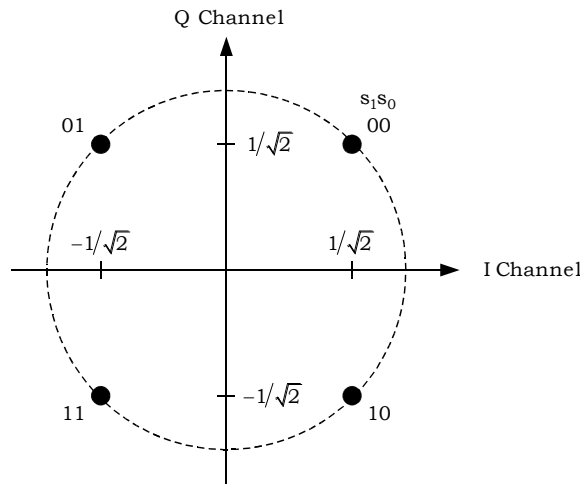
1 1.3.1.3.6.2 QPSK Modulation

2 For physical layer packets using QPSK modulation, two successive channel interleaver  
 3 output symbols shall be grouped to form QPSK modulation symbols. Each group of two  
 4 adjacent interleaver output symbols,  $x(2k)$  and  $x(2k + 1)$ ,  $k = 0, \dots, M - 1$  shall be mapped  
 5 into a complex modulation symbol  $(m_I(k), m_Q(k))$  as specified in Table 1.4.1.3.2.3.5.1-1.  
 6 Figure 1.3.1.3.6.2-1 shows the signal constellation of the QPSK modulator, where  $s_0 = x(2k)$   
 7 and  $s_1 = x(2k + 1)$ .

8 **Table 1.3.1.3.6.2-1. QPSK Modulation Table**

Interleaved Symbols		Modulation Symbols	
$s_1$ $x(2k + 1)$	$s_0$ $x(2k)$	$m_I(k)$	$m_Q(k)$
0	0	D	D
0	1	-D	D
1	0	D	-D
1	1	-D	-D

Note:  $D = 1/\sqrt{2}$ .



11 **Figure 1.3.1.3.6.2-1. Signal Constellation for QPSK Modulation**

12 1.3.1.3.6.3 8-PSK Modulation

13 For physical layer packets using 8-PSK modulation, three successive channel interleaver  
 14 output symbols shall be grouped to form 8-PSK modulation symbols. Each group of three  
 15 adjacent interleaver output symbols,  $x(3k)$ ,  $x(3k + 1)$ , and  $x(3k + 2)$ ,  $k = 0, \dots, M - 1$  shall be  
 16 mapped into a complex modulation symbol  $(m_I(k), m_Q(k))$  as specified in Table  
 17

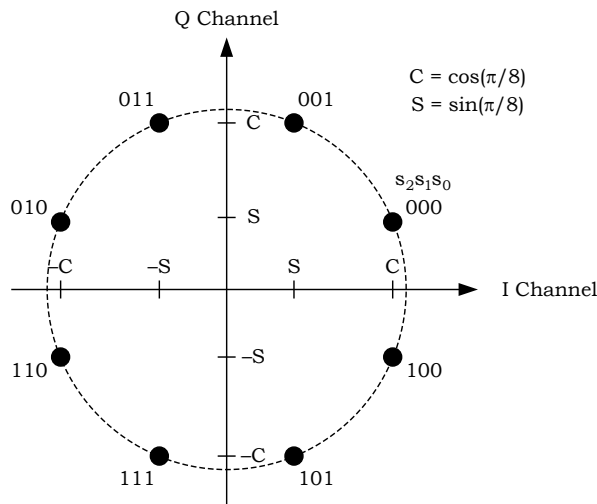
1 1.3.1.3.6.3-1. Figure 1.3.1.3.6.3-1 shows the signal constellation of the 8-PSK modulator,  
 2 where  $s_0 = x(3k)$ ,  $s_1 = x(3k + 1)$ , and  $s_2 = x(3k + 2)$ .

3 **Table 1.3.1.3.6.3-1. 8-PSK Modulation Table**

Interleaved Symbols			Modulation Symbols	
$s_2$ $x(3k + 2)$	$s_1$ $x(3k + 1)$	$s_0$ $x(3k)$	$m_I(k)$	$m_Q(k)$
0	0	0	C	S
0	0	1	S	C
0	1	1	-S	C
0	1	0	-C	S
1	1	0	-C	-S
1	1	1	-S	-C
1	0	1	S	-C
1	0	0	C	-S

Note:  $C = \cos(\pi/8) \approx 0.9239$  and  $S = \sin(\pi/8) \approx 0.3827$ .

4



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6 **Figure 1.3.1.3.6.3-1. Signal Constellation for 8-PSK Modulation**

7 1.3.1.3.6.4 16-QAM Modulation

8 For physical layer packets using 16-QAM modulation, four successive channel interleaver  
 9 output symbols shall be grouped to form 16-QAM modulation symbols. Each group of four  
 10 adjacent interleaver output symbols,  $x(4k)$ ,  $x(4k + 1)$ ,  $x(4k + 2)$ , and  $x(4k + 3)$ ,  $k = 0, \dots, M -$   
 11  $1$  shall be mapped into a complex modulation symbol  $(m_I(k), m_Q(k))$  as specified in Table

1 1.3.1.3.6.4-1. Figure 1.3.1.3.6.4-1 shows the signal constellation of the 16-QAM modulator,  
 2 where  $s_0 = x(4k)$ ,  $s_1 = x(4k + 1)$ ,  $s_2 = x(4k + 2)$ , and  $s_3 = x(4k + 3)$ .

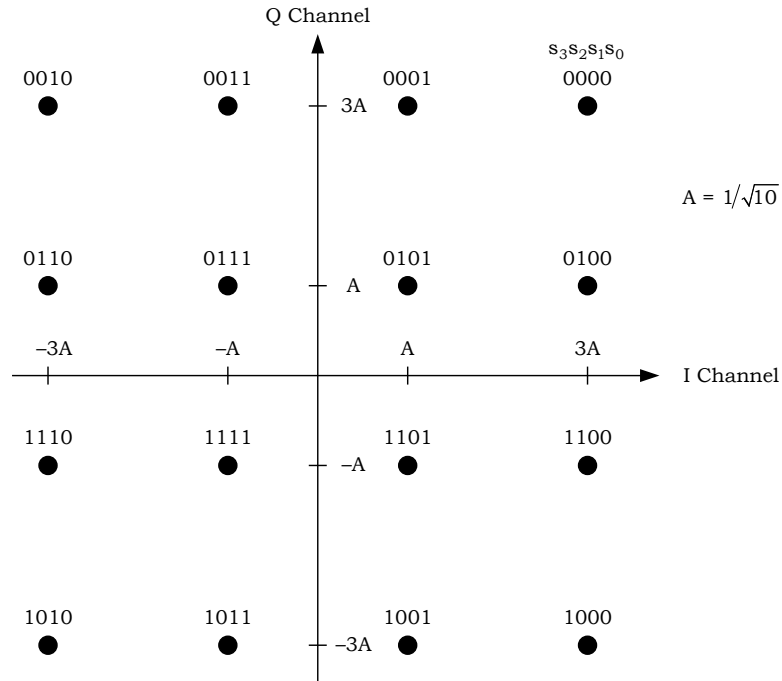
3 **Table 1.3.1.3.6.4-1. 16-QAM Modulation Table**

Interleaved Symbols				Modulation Symbols	
$s_3$ $x(4k + 3)$	$s_2$ $x(4k + 2)$	$s_1$ $x(4k + 1)$	$s_0$ $x(4k)$	$m_Q(k)$	$m_I(k)$
0	0	0	0	3A	3A
0	0	0	1	3A	A
0	0	1	1	3A	-A
0	0	1	0	3A	-3A
0	1	0	0	A	3A
0	1	0	1	A	A
0	1	1	1	A	-A
0	1	1	0	A	-3A
1	1	0	0	-A	3A
1	1	0	1	-A	A
1	1	1	1	-A	-A
1	1	1	0	-A	-3A
1	0	0	0	-3A	3A
1	0	0	1	-3A	A
1	0	1	1	-3A	-A
1	0	1	0	-3A	-3A

Note:  $A = 1/\sqrt{10} \approx 0.3162$ .

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**Figure 1.3.1.3.6.4-1. Signal Constellation for 16-QAM Modulation**

4

1.3.1.3.6.5 64-QAM Modulation

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For physical layer packets using 64-QAM modulation, six successive channel interleaver output symbols shall be grouped to form 64-QAM modulation symbols. Each group of six adjacent interleaver output symbols,  $x(6k)$ ,  $x(6k + 1)$ ,  $x(6k + 2)$ ,  $x(6k+3)$ ,  $x(6k+4)$ , and  $x(6k + 5)$ ,  $k = 0, \dots, M - 1$  shall be mapped into a complex modulation symbol ( $m_I(k)$ ,  $m_Q(k)$ ) as specified in Table 1.3.1.3.6.5-1. Figure 1.3.1.3.6.5-1 shows the signal constellation of the 64-QAM modulator, where  $s_0 = x(6k)$ ,  $s_1 = x(6k + 1)$ ,  $s_2 = x(6k + 2)$ ,  $s_3 = x(6k + 3)$ ,  $s_4 = x(6k + 4)$ , and  $s_5 = x(6k + 5)$ .

12

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**Table 1.3.1.3.6.5-1. 64-QAM Modulation Table**

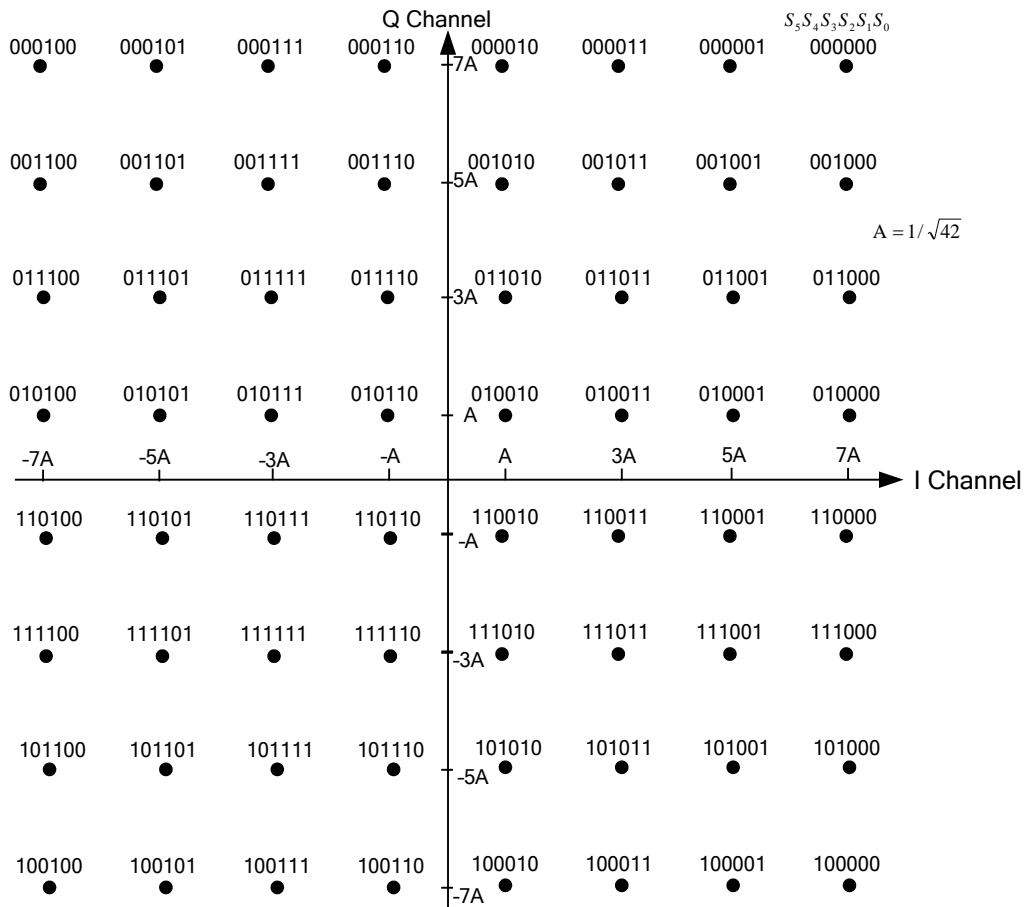
Interleaved Symbols						Modulation Symbols	
$s_5$ $x(6k + 5)$	$s_4$ $x(6k + 4)$	$s_3$ $x(6k + 3)$	$s_2$ $x(6k + 2)$	$s_1$ $x(6k + 1)$	$s_0$ $x(6k)$	$m_Q(k)$	$m_I(k)$
0	0	0	0	0	0	7A	7A
0	0	0	0	0	1	7A	5A
0	0	0	0	1	1	7A	3A
0	0	0	0	1	0	7A	A
0	0	0	1	1	0	7A	-A
0	0	0	1	1	1	7A	-3A
0	0	0	1	0	1	7A	-5A
0	0	0	1	0	0	7A	-7A
0	0	1	0	0	0	5A	7A
0	0	1	0	0	1	5A	5A
0	0	1	0	1	1	5A	3A
0	0	1	0	1	0	5A	A
0	0	1	1	1	0	5A	-A
0	0	1	1	1	1	5A	-3A
0	0	1	1	0	1	5A	-5A
0	0	1	1	0	0	5A	-7A
0	1	1	0	0	0	3A	7A
0	1	1	0	0	1	3A	5A
0	1	1	0	1	1	3A	3A
0	1	1	0	1	0	3A	A
0	1	1	1	1	0	3A	-A
0	1	1	1	1	1	3A	-3A
0	1	1	1	0	1	3A	-5A
0	1	1	1	0	0	3A	-7A
0	1	0	0	0	0	A	7A
0	1	0	0	0	1	A	5A
0	1	0	0	1	1	A	3A
0	1	0	0	1	0	A	A
0	1	0	1	1	0	A	-A

Interleaved Symbols						Modulation Symbols	
$s_5$ $x(6k + 5)$	$s_4$ $x(6k + 4)$	$s_3$ $x(6k + 3)$	$s_2$ $x(6k + 2)$	$s_1$ $x(6k + 1)$	$s_0$ $x(6k)$	$m_Q(k)$	$m_I(k)$
0	1	0	1	1	1	A	-3A
0	1	0	1	0	1	A	-5A
0	1	0	1	0	0	A	-7A
1	1	0	0	0	0	-A	7A
1	1	0	0	0	1	-A	5A
1	1	0	0	1	1	-A	3A
1	1	0	0	1	0	-A	A
1	1	0	1	1	0	-A	-A
1	1	0	1	1	1	-A	-3A
1	1	0	1	0	1	-A	-5A
1	1	0	1	0	0	-A	-7A
1	1	1	0	0	0	-3A	7A
1	1	1	0	0	1	-3A	5A
1	1	1	0	1	1	-3A	3A
1	1	1	0	1	0	-3A	A
1	1	1	1	1	0	-3A	-A
1	1	1	1	1	1	-3A	-3A
1	1	1	1	0	1	-3A	-5A
1	1	1	1	0	0	-3A	-7A
1	0	1	0	0	0	-5A	7A
1	0	1	0	0	1	-5A	5A
1	0	1	0	1	1	-5A	3A
1	0	1	0	1	0	-5A	A
1	0	1	1	1	0	-5A	-A
1	0	1	1	1	1	-5A	-3A
1	0	1	1	0	1	-5A	-5A
1	0	1	1	0	0	-5A	-7A
1	0	0	0	0	0	-7A	7A
1	0	0	0	0	1	-7A	5A
1	0	0	0	1	1	-7A	3A

Interleaved Symbols						Modulation Symbols	
$s_5$ $x(6k + 5)$	$s_4$ $x(6k + 4)$	$s_3$ $x(6k + 3)$	$s_2$ $x(6k + 2)$	$s_1$ $x(6k + 1)$	$s_0$ $x(6k)$	$m_Q(k)$	$m_I(k)$
1	0	0	0	1	0	-7A	A
1	0	0	1	1	0	-7A	-A
1	0	0	1	1	1	-7A	-3A
1	0	0	1	0	1	-7A	-5A
1	0	0	1	0	0	-7A	-7A

Note:  $A = 1/\sqrt{42} \approx 0.1543$ .

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**Figure 1.3.1.3.6.5-1. Signal Constellation for 64-QAM Modulation**

5

1.3.1.3.7 Modulation Symbol Puncturing and Repetition

6

Each frame is encoded and interleaved separately except for the frames corresponding to

7

data rates 640 bps and 1280 bps. For 6.4 kHz channel assignment, total 96 modulation

1 symbols are generated from the channel interleaver output. The first 94 modulation  
 2 symbols shall be transmitted in a frame and the remaining 2 symbols shall be discarded  
 3 (punctured). For 12.8 kHz channel assignment, total 192 modulation symbols are  
 4 generated. The first 188 modulation symbols shall be transmitted in a frame and the  
 5 remaining 4 symbols shall be discarded (punctured).

6 For 256-bit physical layer packet corresponding to 640 bps data rate that spans 20 frames,  
 7 encoding and interleaving block consist of the entire packet. Using rate 1/5 turbo code, 256  
 8 input bits are encoded to 1280 code bits and then channel interleaved. Total of 1280 BPSK  
 9 modulation symbols are generated from the channel interleaver outputs. The first 600  
 10 symbols out of 1280 shall be repeated and appended at the end of the block, resulting in a  
 11 total of 1880 symbols to be transmitted over 20 frames (94 symbols per frame).

12 For 256-bit physical layer packet corresponding to 1.28 kbps data rate that spans 10  
 13 frames, encoding and interleaving block consist of the entire packet. Using rate 4/15 turbo  
 14 code, 256 input bits are encoded and then channel interleaved. Total of 940 BPSK  
 15 modulation symbols are generated from the channel interleaver outputs which shall be  
 16 transmitted over 10 frames (94 symbols per frame).

#### 17 1.3.1.3.8 PN Quadrature Covering

18 The modulated symbols shall be covered with a PN sequence. The PN sequences used for  
 19 covering are generated using a pair of access terminal common short PN sequence and a  
 20 pair of masks MI and MQ. The access terminal common short PN sequences shall be based  
 21 on the following characteristic polynomials, respectively:

$$22 P_I(x) = x^{12} + x^6 + x^4 + x + 1$$

23 (for the in-phase (I) channel)

24 and

$$25 P_Q(x) = x^{12} + x^9 + x^3 + x^2 + 1$$

26 (for the quadrature-phase (Q) channel).

27 The maximum length linear feedback shift-register sequence  $\{I(n)\}$  and  $\{Q(n)\}$  based on the  
 28 above are of length  $2^{12}-1=4095$  and can be generated by the following linear recursions:

$$29 I(n)=I(n-12) \oplus I(n-11) \oplus I(n-8) \oplus I(n-6)$$

30 (based on  $P_I(x)$  as the characteristic polynomial)

31 and

$$32 Q(n)= Q(n-12) \oplus Q(n-10) \oplus I(n-9) \oplus I(n-3)$$

33 (based on  $P_Q(x)$  as the characteristic polynomial),

34 where  $I(n)$  and  $Q(n)$  are binary valued ('0' and '1') and the additions are modulo-2. A frame  
 35 has 112 and 224 symbols to be covered for 1 and 2 channel assignment, respectively. At  
 36 the boundary of every 80 ms (48 slots), i.e. at the CDMA time T that satisfies

$$37 (T- \text{FrameOffset}) \bmod 48 = 0$$

1 where both time T and FrameOffset are in units of slot, the common short PN sequence  
 2 generator shall be reloaded with the following initial state:

3 I channel: the first 12 outputs should be 1000 0000 0000 (MSB output first)

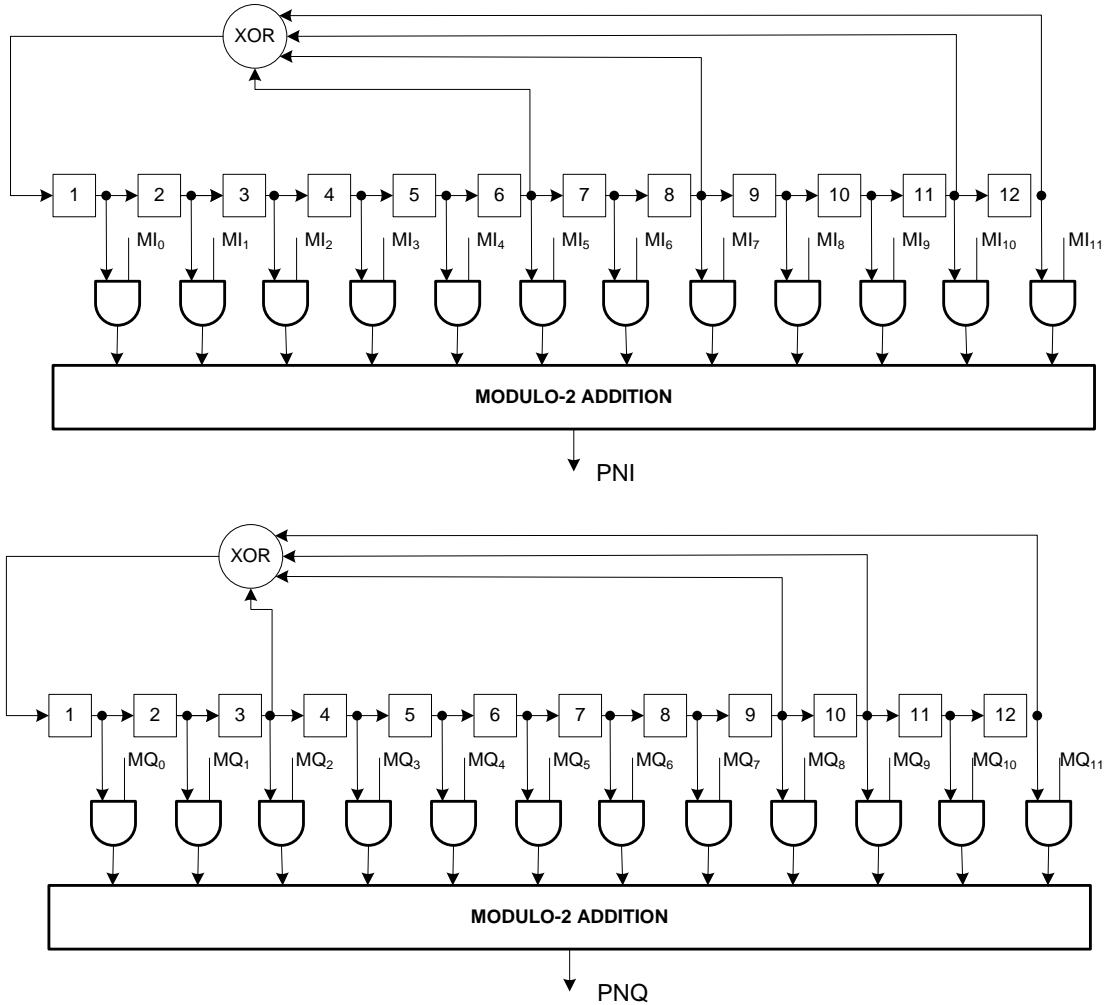
4 Q channel: the first 12 outputs should be 0101 0101 0101 (MSB output first)

5 A pair of 12-bit masks, MI and MQ, shall be applied to the above short PN sequences. The  
 6 masks depend on the channel (i.e., Access or Traffic) on which the access terminal is  
 7 transmitting.

8 To transmit on the Access channel, the 12-bit masks MI and MQ shall be determined as  
 9 follows. Bits MI<sub>3</sub> to MI<sub>0</sub> and MQ<sub>3</sub> to MQ<sub>0</sub> shall be set to the lower 4 bits of assigned channel  
 10 number. Bits MI<sub>11</sub> to MI<sub>4</sub> shall be set equal to the result of (A<sub>31</sub> to A<sub>24</sub>) ⊕ (A<sub>23</sub> to A<sub>16</sub>) ⊕  
 11 (A<sub>15</sub> to A<sub>8</sub>) ⊕ (A<sub>7</sub> to A<sub>0</sub>), where A<sub>23</sub> to A<sub>0</sub> are lower 24 bits of 42-bit access long code mask  
 12 MI<sub>ACMAC</sub> (given as public data of the Access Channel MAC Protocol). Similarly, Bits MQ<sub>11</sub> to  
 13 MQ<sub>4</sub> shall be set to the result of (B<sub>31</sub> to B<sub>24</sub>) ⊕ (B<sub>23</sub> to B<sub>16</sub>) ⊕ (B<sub>15</sub> to B<sub>8</sub>) ⊕ (B<sub>7</sub> to B<sub>1</sub>, B<sub>32</sub>),  
 14 where B<sub>23</sub> to B<sub>0</sub> are lower 24 bits of 42-bit access long code mask MQ<sub>ACMAC</sub> (given as public  
 15 data of the Access Channel MAC Protocol) and B<sub>32</sub> is 33<sup>th</sup> bit of MQ<sub>ACMAC</sub>. If the above  
 16 operation results in all zero mask, the mask shall be set to one “1” (MSB) followed by eleven  
 17 “0”s.

18 To transmit on the Reverse Traffic Channel, the masks MI and MQ shall be set to the lower  
 19 12 bits of the 42-bit user specific long code masks, MI<sub>RTCMAC</sub> and MQ<sub>RTCMAC</sub> (given as public  
 20 data of the Reverse Traffic Channel MAC Protocol), respectively. When the lower 12 bits of  
 21 the 42 bit long code mask are all “0”s, the mask shall be set to one “1” (MSB) followed by  
 22 eleven “0”s.

23 Figure 1.3.1.3.8-1 shows the details of PN generation and masking.



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**Figure 1.3.1.3.8-1. PN Sequence Generator**

3 1.3.1.3.9 Baseband Filtering

4 The complex modulated symbols shall be baseband filtered by a square-root raised-cosine  
5 pulse filter with 14.286% excess bandwidth. The impulse response of the pulse filter  $x(t)$  is  
6 given by the following equation:

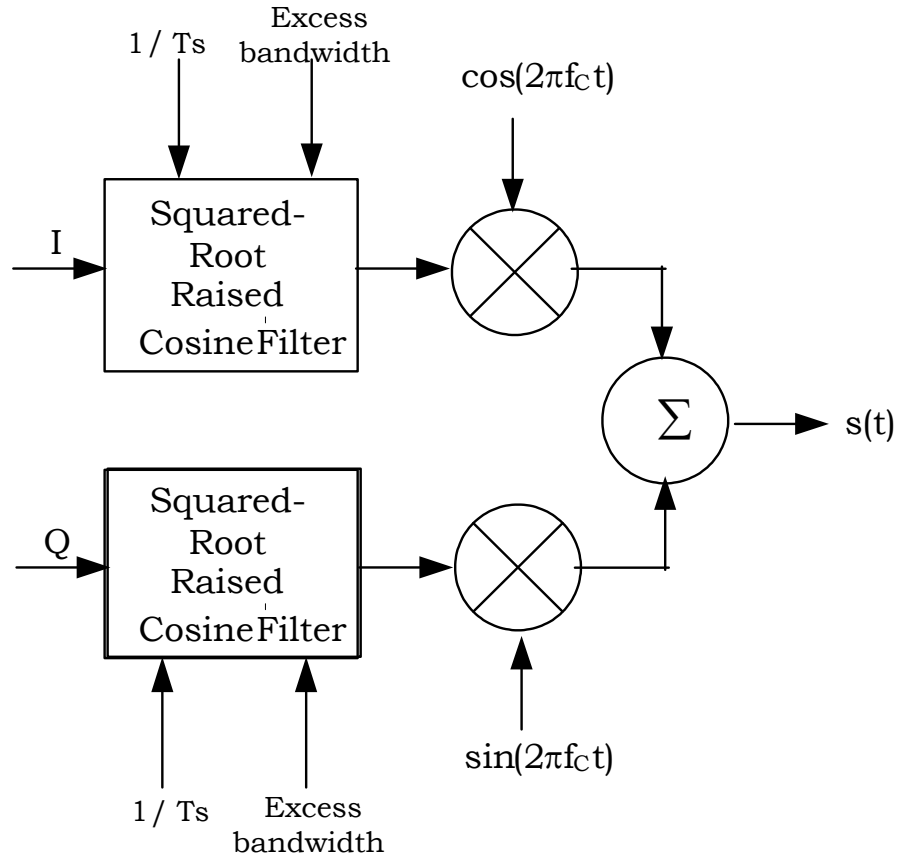
7

$$x(t) = 8\beta \frac{\cos\left[(1+\beta)\pi\frac{t}{T_s}\right] + \frac{\sin\left[(1-\beta)\pi\frac{t}{T_s}\right]}{4\beta\frac{t}{T_s}}}{\left[1 - \left(4\beta\frac{t}{T_s}\right)^2\right]}$$

8 where  $\beta = (6.4/5.6-1) = 0.14286$  is the excess bandwidth and  $T_s$  is the duration of a  
9 modulation symbol. The modulation symbol rate is 5.6 kbaud or 11.2 kbaud, depending

1 on 6.4 kHz or 12.8 kHz channel assigned, respectively. The outputs of the baseband filters  
 2 shall be modulated to the center-frequency of the narrowband channel.

3  
 4



5  
 6

**Figure 1.3.1.3.9-1. Baseband Filtering and Transmission of Narrowband Channel**

7 1.3.2 Receiver

8 1.3.2.1 Closed-Loop Power-Control Operation

9 The access terminal shall employ both power control and data rate control on the reverse  
 10 link. The objective of the power control is to regulate the transmit power of the access  
 11 terminal while maintaining a given quality of service, which is usually benchmarked by the  
 12 frame error rate. The data rate control is embedded in the power control. The access  
 13 terminal determines a suitable reverse data rate depending on its PA headroom and the  
 14 bandwidth requirements of different applications. Power and rate control is a combination  
 15 of mechanisms that continually adjust transmit power and data rate so as to satisfy the  
 16 quality of service requirement under varying channel and loading conditions.

17 Once the connection is established, the access network transmits '0' (up) or '1' (down) RPC  
 18 bits to the access terminal, based on measurements of the reverse link signal quality. If the

1 received quality is above the target threshold, a '1' bit is transmitted. If the received quality  
2 is below the target threshold, a '0' bit is transmitted.

3 The access terminal shall receive RPC commands in slots T as specified by the following  
4 equation:

$$(T - \text{FrameOffset}) \bmod 12 = 7,$$

6 where T is the CDMA System Time in slots.

7 The access terminal shall adjust its transmit power and/or data rate based on the power  
8 control commands it receives. Based on its PA headroom, the access terminal shall increase  
9 its transmit power and/or decrease its data rate when a power up command is received,  
10 whereas it shall decrease its transmit power and/or increase its data rate when a power  
11 down command is received.

### 12 1.3.2.2 Closed Loop Frequency Control Operation

13 The access terminal shall use the Reverse Link Frequency Control Channel for closed loop  
14 correction of its frequency error. The access network transmits '0' (up) and '1' (down) RFC  
15 bits to the access terminal, based on the measurement of the reverse link frequency error.  
16 If the measured frequency error is positive and above the target threshold, a '1' bit is  
17 transmitted. If the measured frequency error is negative and below the target threshold, a  
18 '0' bit is transmitted. RFC bits are time-multiplexed with RPC bits on the same MAC  
19 channel.

20 The access terminal shall receive RFC commands in slots T as specified by the following  
21 equation:

$$(T - \text{FrameOffset}) \bmod 12 = 3,$$

23 where T is the CDMA System Time in slots.

24 If the received RFC bit is '0' the access terminal shall increase its transmission frequency  
25 by 0.5 Hz. If the received RFC bit is '1' the access terminal shall decrease its transmission  
26 frequency by 0.5 Hz.

### 27 1.3.3 Synchronization and Timing

28 The nominal relationship between the access terminal and access network transmit and  
29 receive time references shall be as shown in Figure 1.14-1 of [1]. The access terminal shall  
30 establish a time reference that is used to derive timing for the transmitted chips, symbols,  
31 slots, frames, and system timing. The access terminal initial time reference shall be  
32 established from the acquired Pilot Channel and from the Sync message transmitted on the  
33 Control Channel. Under steady-state conditions, the access terminal time reference shall be  
34 within  $\pm 1 \mu\text{s}$  of the time of occurrence, as measured at the access terminal antenna  
35 connector, of the earliest arriving multipath component being used for demodulation. If  
36 another multipath component belonging to the same Pilot Channel or to a different Pilot  
37 Channel becomes the earliest arriving multipath component to be used, the access terminal  
38 time reference shall track to the new component. If the difference between the access  
39 terminal time reference and the time of occurrence of the earliest arriving multipath  
40 component being used for demodulation, as measured at the access terminal antenna

1 connector, is less than  $\pm 1 \mu\text{s}$ , the access terminal may directly track its time reference to  
2 the earliest arriving multipath component being used for demodulation.

3 If an access terminal time reference correction is needed, it shall be corrected no faster  
4 than 203 ns (1/4 chip) in any 200-ms period and no slower than 305 ns (3/8 PN chip) per  
5 second.

6 The access terminal time reference shall be used as the transmit time reference of the  
7 Reverse Traffic Channel and the Access Channel.

8

## 1.4 Access Network Requirements

This section defines requirements specific to access network equipment and operation.

### 1.4.1 Transmitter

The transmitter shall reside in each sector of the access network. These requirements apply to the transmitter in each sector.

#### 1.4.1.1 Frequency Parameters

The access network shall meet the requirements in the current version of [23].

##### 1.4.1.1.1 Frequency Tolerance

The average frequency difference between the actual sector transmit carrier frequency and the specified sector transmit frequency assignment shall be less than  $\pm 5 \times 10^{-8}$  of the frequency assignment ( $\pm 0.05$  ppm).

#### 1.4.1.2 Power Output Characteristics

The access network shall meet the requirements in the current version of [12].

#### 1.4.1.3 Modulation Characteristics

##### 1.4.1.3.1 Forward Channel Structure

The Forward Channel shall have the overall structure shown in Figure 1.4.1.3.1-1. The Forward Channel shall consist of the following time-multiplexed channels: the Pilot Channel, the Forward Medium Access Control (MAC) Channel, and the Forward Traffic Channel or the Control Channel. The Traffic Channel carries user physical layer packets. The Control Channel carries control messages, and it may also carry user traffic. Each channel is further decomposed into code-division-multiplexed quadrature Walsh channels.

The forward link shall consist of slots of length 2048 chips (1.66... ms). Groups of 16 slots shall be aligned to the PN rolls of the zero-offset PN sequences and shall align to CDMA System Time on even-second ticks.

Within each slot, the Pilot, MAC, and Traffic or Control Channels shall be time-division multiplexed as shown in Figure 1.4.1.3.1-2 and shall be transmitted at the same power level.

The Pilot Channel shall consist of all-'0' symbols transmitted on the I-branch with Walsh cover 0. Each slot shall be divided into two half slots, each of which contains a pilot burst. Each pilot burst shall have a duration of 96 chips and be centered at the midpoint of the half slot.<sup>6</sup>

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<sup>6</sup> The pilot is used by the access terminal for initial acquisition, phase recovery, timing recovery, and maximal-ratio combining. An additional function of the pilot is to provide the access terminal with a means of predicting the receive C/I for the purpose of access-terminal-directed forward data rate control (DRC) of the Data Channel transmission.

1 The MAC Channel shall consist of two subchannels: the Reverse Power Control (RPC)  
2 Channel and the Reverse Frequency Control (RFC) Channel. The RPC Channel transmits  
3 power control commands used by the access terminal for closed loop power control. The  
4 RFC Channel transmits frequency control command used by the access terminal for closed  
5 loop frequency control. Each MAC Channel symbol shall be BPSK or OOK modulated on the  
6 in-phase or quadrature-phase of one of 128 128-ary Walsh codewords (covers). The MAC  
7 symbol Walsh covers shall be transmitted two times per slot in four bursts of 64 chips  
8 each. A burst shall be transmitted immediately preceding each of the pilot bursts in a slot,  
9 and a burst shall be transmitted immediately following each of the pilot bursts in a slot.  
10 The Walsh channel gains may vary the relative power.

11 The Forward Traffic Channel is a packet-based, variable-rate channel. The user physical  
12 layer packets for an access terminal shall be transmitted at a data rate that varies from 4.8  
13 kbps to 3.072 Mbps.<sup>7</sup> Forward Traffic Channel and Control Channel physical layer packets  
14 are defined using a Transmission Format. The Transmission Format consists of the  
15 following:

- 16 • Physical Layer Packet Size of the physical layer packet (in bits)
- 17 • Nominal Transmit Duration of the physical layer packet (in slots)
- 18 • Preamble Length associated with the physical layer packet (in chips)

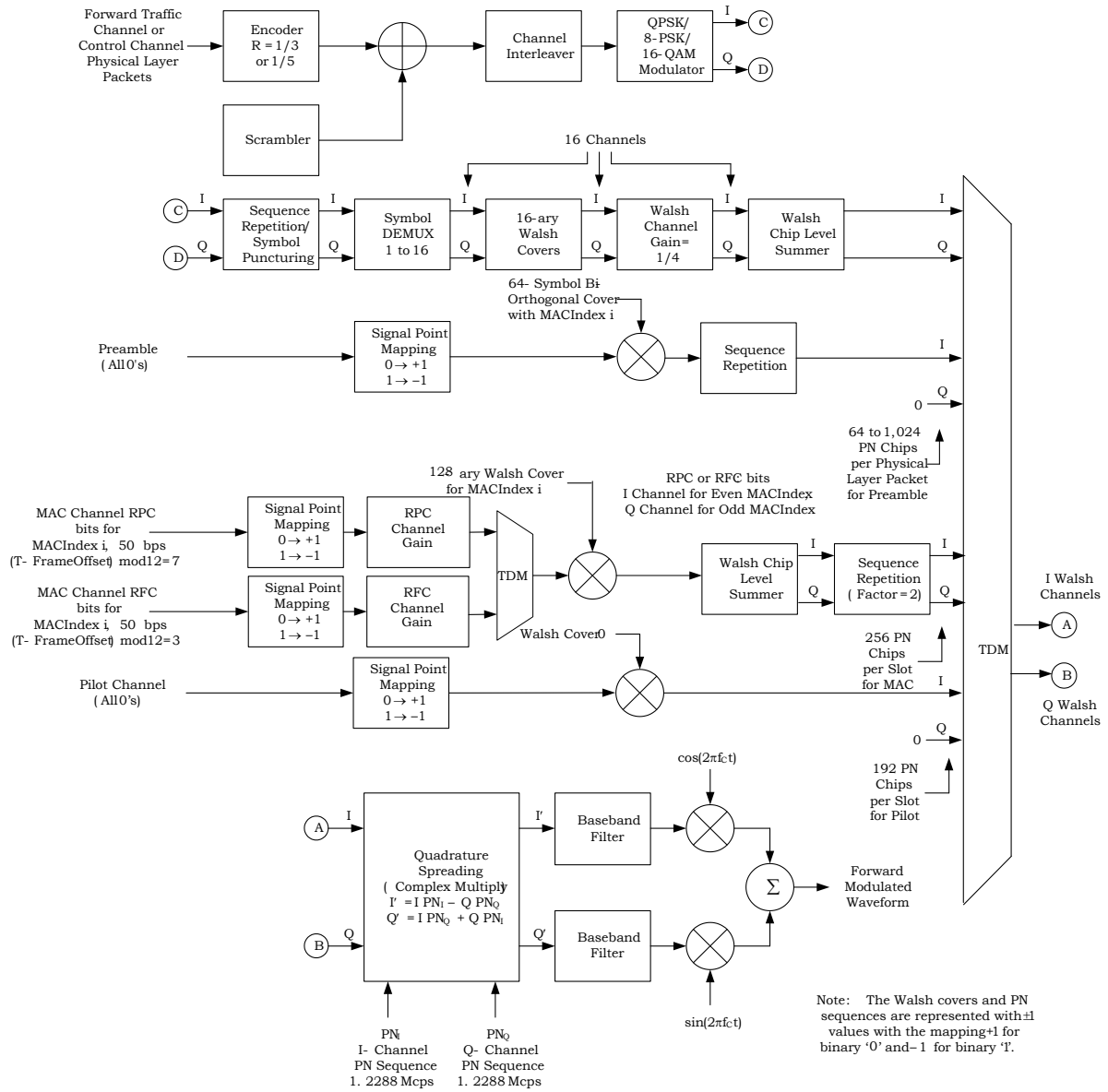
19 The Transmission Format is public data of the Forward Traffic Channel MAC Protocol. For  
20 example, (1024, 1, 64) indicates a 1024-bit physical layer packet with a nominal transmit  
21 duration of 1 slot with a 64-chip preamble.

22 The Forward Traffic Channel and Control Channel data shall be encoded in blocks called  
23 physical layer packets. The output of the encoder shall be scrambled and then fed into a  
24 channel interleaver. The output of the channel interleaver shall be fed into a QPSK/8-  
25 PSK/16-QAM modulator. The modulated symbol sequences shall be repeated and  
26 punctured, as necessary. Then, the resulting sequences of modulation symbols shall be  
27 demultiplexed to form 16 pairs (in-phase and quadrature) of parallel streams. Each parallel  
28 stream with a rate of 76.8 ksps is covered with a distinct Walsh function of length 16. The  
29 Walsh-coded symbols of all the streams shall be summed together to form a single in-phase  
30 stream and a single quadrature stream at a chip rate of 1.2288 Mcps. The resulting chips  
31 are time-division multiplexed with the preamble, Pilot Channel, and MAC Channel chips to  
32 form the resultant sequence of chips for the quadrature spreading operation. Forward  
33 Traffic Channel and Control Channel physical layer packets can be transmitted in 1 to 16  
34 slots (see Table 1.4.1.3.1.1-1). When more than one slot is allocated, the transmit slots  
35 shall use 4-slot interlacing. That is, the transmit slots of a physical layer packet shall be  
36 separated by three intervening slots, and slots of other physical layer packets shall be  
37 transmitted in the slots between those transmit slots. For example, the 153.6 kbps Forward  
38 Traffic Channel physical layer packet with Transmission Format (1024, 4, 256) uses four  
39 slots, and these slots are transmitted with a three-slot interval between them. The slots  
40 from other physical layer packets are interlaced in the three intervening slots.

---

<sup>7</sup> The CQI symbol from the access terminal is based primarily on its estimate of the forward C/I for the duration of the next possible forward link packet transmission.

- 1 When the access network has transmitted all the slots of a physical layer packet, the
- 2 physical layer shall return a *ForwardTrafficCompleted* indication.
- 3 The Control Channel shall be transmitted using the Transmission Formats of (128, 4,
- 4 1024), (256, 4, 1024), (512, 4, 1024), (1024, 16, 1024), and (1024, 8, 512). The modulation
- 5 characteristics for the Control Channel shall be the same as those of the Forward Traffic
- 6 Channel transmitted using the corresponding Transmission Format.
- 7 The Forward Traffic Channel and Control Channel data symbols shall fill the slot as shown
- 8 in Figure 1.4.1.3.1-2. A slot during which no traffic or control data is transmitted is
- 9 referred to as an idle slot. During an idle slot, the sector shall transmit the Pilot Channel
- 10 and the MAC Channel, as described earlier.

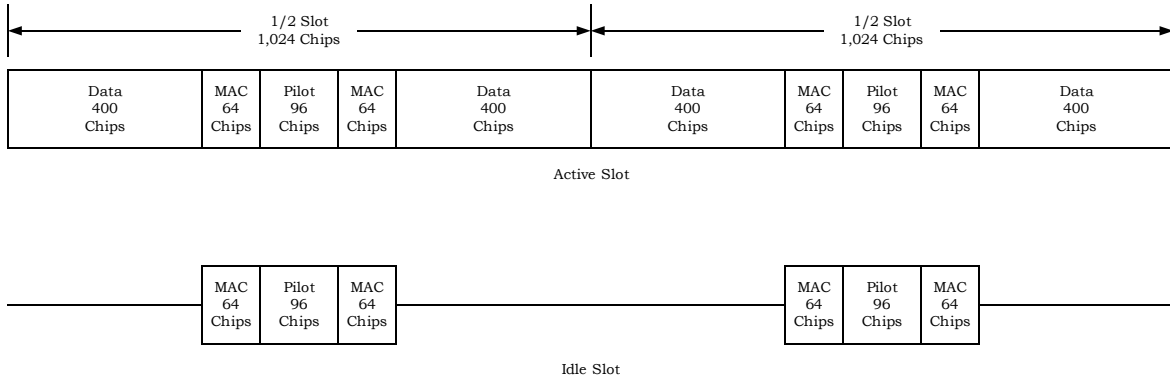


11

12

**Figure 1.4.1.3.1-1. Forward Channel Structure**

13



1  
2  
3  
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7

**Figure 1.4.1.3.1-2. Forward Link Slot Structure**

1.4.1.3.1.1 Modulation Parameters

The modulation parameters for the Forward Traffic Channel and the Control Channel shall be as shown in Table 1.4.1.3.1.1-1. The Control Channel shall only use the Transmission Formats of (1024, 8, 512), (1024, 16, 1024), (128, 4, 1024), (256, 4, 1024), or (512, 4, 1024).

1 **Table 1.4.1.3.1.1-1. Modulation Parameters for the Forward Traffic Channel and the**  
 2 **Control Channel**

<b>Transmission Format (Physical Layer Packet Size (bits), Nominal Transmit Duration (slots), Preamble Length (chips))</b>	<b>Code Rate</b>	<b>Modulation Type</b>	<b>Nominal Data Rate (kbps)</b>
(128, 16, 1024)	1/5	QPSK	4.8
(128, 8, 512)	1/5	QPSK	9.6
(128, 4, 1024)	1/5	QPSK	19.2
(128, 4, 256)	1/5	QPSK	19.2
(128, 2, 128)	1/5	QPSK	38.4
(128, 1, 64)	1/5	QPSK	76.8
(256, 16, 1024)	1/5	QPSK	9.6
(256, 8, 512)	1/5	QPSK	19.2
(256, 4, 1024)	1/5	QPSK	38.4
(256, 4, 256)	1/5	QPSK	38.4
(256, 2, 128)	1/5	QPSK	76.8
(256, 1, 64)	1/5	QPSK	153.6
(512, 16, 1024)	1/5	QPSK	19.2
(512, 8, 512)	1/5	QPSK	38.4
(512, 4, 1024)	1/5	QPSK	76.8
(512, 4, 256)	1/5	QPSK	76.8
(512, 4, 128)	1/5	QPSK	76.8
(512, 2, 128)	1/5	QPSK	153.6
(512, 2, 64)	1/5	QPSK	153.6
(512, 1, 64)	1/5	QPSK	307.2
(1024, 16, 1024)	1/5	QPSK	38.4
(1024, 8, 512)	1/5	QPSK	76.8
(1024, 4, 256)	1/5	QPSK	153.6
(1024, 4, 128)	1/5	QPSK	153.6
(1024, 2, 128)	1/5	QPSK	307.2
(1024, 2, 64)	1/5	QPSK	307.2
(1024, 1, 64)	1/3	QPSK	614.4
(2048, 4, 128)	1/3	QPSK	307.2
(2048, 2, 64)	1/3	QPSK	614.4

<b>Transmission Format (Physical Layer Packet Size (bits), Nominal Transmit Duration (slots), Preamble Length (chips))</b>	<b>Code Rate</b>	<b>Modulation Type</b>	<b>Nominal Data Rate (kbps)</b>
(2048, 1, 64)	1/3	QPSK	1,228.8
(3072, 2, 64)	1/3	8-PSK	921.6
(3072, 1, 64)	1/3	8-PSK	1,843.2
(4096, 2, 64)	1/3	16-QAM	1,228.8
(4096, 1, 64)	1/3	16-QAM	2,457.6
(5120, 2, 64)	1/3	16-QAM	1,536.0
(5120, 1, 64)	1/3	16-QAM	3,072.0

1 The modulation parameters for the MAC Channel shall be as shown in Table 1.4.1.3.1.1-2.

2 **Table 1.4.1.3.1.1-2. Modulation Parameters for the MAC Channel**

<b>Parameter</b>	<b>RPC Channel</b>	<b>RFC Channel</b>
Rate(bps)	50	50
Bit Repetition Factor	1	1
Modulation (Channel)	BPSK(I or Q)	BPSK(I or Q)
Modulation Symbol Rate (sps)	100	100
Walsh Cover Length	128	128
Walsh Sequence Repetition Factor	2	2
PN Chips/Slot	256	256
PN Chips/Bit	256	256

3 1.4.1.3.1.2 Data Rates

4 The Forward Traffic Channel shall support variable-data-rate transmission from 4.8 kbps  
5 to 3.072 Mbps corresponding to the Transmission Formats of (128, 16, 1024) and (5120, 1,  
6 64) respectively, as shown in Table 1.4.1.3.1.1-1

7 The data rate of the Control Channel shall be 76.8 kbps (Transmission Format of (512, 4,  
8 1024) or (1024, 8, 512)), 38.4 kbps (Transmission Format of (256, 4, 1024) or (1024, 16,  
9 1024)), or 19.2 kbps (Transmission Format of (128, 4, 1024)).

1 1.4.1.3.2 Forward Link Channels

2 1.4.1.3.2.1 Pilot Channel

3 A Pilot Channel shall be transmitted by the sector on each active Forward Channel as  
 4 described in 1.4.1.3.1. The Pilot Channel is an unmodulated signal that is used for  
 5 synchronization and other functions by an access terminal operating within the coverage  
 6 area of the sector. The Pilot Channel shall be transmitted at the full sector power.

7 1.4.1.3.2.1.1 Modulation

8 The Pilot Channel shall consist of all-'0' symbols transmitted on the I component only.

9 1.4.1.3.2.1.2 Orthogonal Spreading

10 The Pilot Channel shall be assigned Walsh cover 0.

11 1.4.1.3.2.1.3 Quadrature Spreading

12 See 1.4.1.3.4.

13 1.4.1.3.2.2 Forward MAC Channel

14 The Forward MAC Channel shall be composed of Walsh channels that are orthogonally  
 15 covered and BPSK modulated or OOK (ON-OFF Keying) modulated on each phase of the  
 16 carrier (either in-phase or quadrature phase). Each Walsh channel shall be identified by a  
 17 MACIndex value that is between 0 and 127 and defines a unique 128-ary Walsh cover and  
 18 a unique modulation phase. The Walsh functions assigned to the MACIndex values shall be  
 19 as shown in Table 1.4.1.3.2.2-1.

20 **Table 1.4.1.3.2.2-1. Forward Link MAC Channel Assignment**

MAC Index, i	128-ary Walsh Function	(T – FrameOffset) mod 12 = 7 or 3		(T – FrameOffset) mod 12 ≠ 7 or 3	
		I-branch	Q-branch	I-branch	Q-branch
6, 8, ..., 62	$W_{i/2}^{128}$	RPC/RFC	Not Used	Not Used	Not Used
5 (if broadcast is not negotiated), 7, 9, ..., 63	$W_{(i-1)/2+32}^{128}$	Not Used	RPC/RFC	Not Used	Not Used
72,74,....,126	$W_{i/2+32}^{128}$	RPC/RFC	Not Used	Not Used	Not Used
73,75,....,127	$W_{(i-1)/2+64}^{128}$	Not Used	RPC/RFC	Not Used	Not Used
4	$W_2^{128}$	Not Used		Not Used	

21

1 RPC/RFC Channels with even-numbered MACIndex values shall be assigned to the in-  
2 phase (I) modulation phase, while those with odd-numbered MACIndex values shall be  
3 assigned to the quadrature (Q) modulation phase.

4 RPC Channels shall be transmitted in slots T specified by the following equation:

$$5 \quad (T - \text{FrameOffset}) \bmod 12 = 7,$$

6 where T is the CDMA System Time in slots.

7 RFC Channels shall be transmitted in slots T specified by the following equation:

$$8 \quad (T - \text{FrameOffset}) \bmod 12 = 3,$$

9 where T is the CDMA System Time in slots.

10

11 The MAC symbol Walsh covers shall be transmitted two times per slot in four bursts of  
12 length 64 chips each. These bursts shall be transmitted immediately preceding and  
13 following the pilot bursts of each slot.

14 The MAC Channel use versus MACIndex shall be as specified in Table 1.4.1.3.2.2-2.

15 Symbols of each MAC Channel shall be transmitted on one of the Walsh channels. The  
16 MAC channel gains may vary the relative power as a function of time. The orthogonal Walsh  
17 channels shall be scaled to maintain a constant total transmit power. The Walsh channel  
18 gains can vary as a function of time.

1

**Table 1.4.1.3.2.2-2. MAC Channel and Preamble Use Versus MACIndex**

<b>MACIndex</b>	<b>MAC Channel Use</b>	<b>Preamble Use</b>	<b>Preamble Length</b>
0 and 1	Not Used	Not Used	N/A
2	Not Used	76.8 kbps Control Channel (1024, 8, 512)	512
3	Not Used	38.4 kbps Control Channel (1024, 16, 1024)	1024
4	Not Used	Not Used	N/A
5	Available for RPC/RFC Channel Transmissions	Forward Traffic Channel if Broadcast is not negotiated	Variable
64 and 65	Not Used	Not Used	N/A
66	Not Used	Multi-User packet (128, 4, 256) (256, 4, 256) (512, 4, 256) (1024, 4, 256)	256
67	Not Used	Multi-User packet (2048, 4, 128)	128
68	Not Used	Multi-User packet (3072, 2, 64)	64
69	Not Used	Multi-User packet (4096, 2, 64)	64
70	Not Used	Multi-User packet (5120, 2, 64)	64
71	Not Used	19.2 kbps Control Channel (128, 4, 1024) 38.4 kbps Control Channel (256, 4, 1024) 76.8 kbps Control Channel (512, 4, 1024)	1024
6-63 and 72-127	Available for RPC/RFC Channel Transmissions	Available for Forward Traffic Channel Transmissions of Single User packets	Variable

2 1.4.1.3.2.2.1 Reverse Power Control Channel

1 The Reverse Power Control (RPC) Channel for each access terminal with an open  
 2 connection shall be assigned to one of the available MAC Channels. It is used for the  
 3 transmission of the RPC bit stream destined to that access terminal. The RPC Channel and  
 4 the RFC Channel shall be transmitted on the in-phase or quadrature-phase of the same  
 5 MAC Channel according to the assignment defined in Table 1.4.1.3.2.2-1. The RPC Channel  
 6 shall be time-division multiplexed with the RFC Channel and transmitted in 1 slot out of  
 7 every 12 slots.

8 The RPC data rate shall be 50 bps. The access network shall transmit an RPC bit in every  
 9 slot T specified using the following equation:

$$(T - \text{FrameOffset}) \bmod 12 = 7,$$

11 where T is the CDMA System Time in slots.

12 Each RPC bit shall be transmitted two times in a slot in four bursts of 64 chips each. These  
 13 bursts shall be transmitted immediately preceding and following each pilot burst in a slot  
 14 as shown in Figure 1.4.1.3.1-2.

#### 15 1.4.1.3.2.2.2 Reverse Frequency Control Channel

16 The Reverse Frequency Control (RFC) Channel for each access terminal with an open  
 17 connection shall be assigned to one of the available MAC Channels. It is used for the  
 18 transmission of the RFC bit stream destined to that access terminal. The RPC Channel and  
 19 the RFC Channel shall be transmitted on the in-phase or quadrature phase of the same  
 20 MAC Channel according to the assignment defined in Table 1.4.1.3.2.2-1. The RFC Channel  
 21 shall be time-division multiplexed with the RPC Channel and transmitted in 1 slot out of  
 22 every 12 slots.

23 The RFC data rate shall be 50 bps. The access network shall transmit an RFC bit in every  
 24 slot T specified using the following equation:

$$(T - \text{FrameOffset}) \bmod 12 = 3,$$

26 where T is the CDMA System Time in slots.

27 Each RFC bit shall be transmitted two times in a slot in bursts of 64 chips each. These  
 28 bursts shall be transmitted immediately preceding and following each pilot burst in a slot  
 29 as shown in Figure 1.4.1.3.1-2. .

#### 30 1.4.1.3.2.3 Forward Traffic Channel

##### 31 1.4.1.3.2.3.1 Forward Traffic Channel Preamble

32 A preamble sequence shall be transmitted with each Forward Traffic Channel and Control  
 33 Channel physical layer packet in order to assist the access terminal with synchronization of  
 34 each variable-rate transmission.

35 The preamble shall consist of all-'0' symbols transmitted on the in-phase component only.  
 36 The preamble shall be time multiplexed into the Forward Traffic Channel stream as  
 37 described in 1.4.1.3.3. The preamble sequence shall be covered by a 64-chip bi-orthogonal  
 38 sequence and the sequence shall be repeated several times depending on the transmit

1 mode. The bi-orthogonal sequence shall be specified in terms of the 64-ary Walsh functions  
 2 and their bit-by-bit complements by

$$3 \quad W_{i/2}^{64} \text{ for } i = 0, 2, \dots, 126$$

$$4 \quad \overline{W_{(i-1)/2}^{64}} \text{ for } i = 1, 3, \dots, 127$$

5 where  $i = 0, 1, \dots, 127$  is the MACIndex value and  $\overline{W_i^{64}}$  is the bit-by-bit complement of the  
 6 64-chip Walsh function of index  $i$ .

7 The channel type versus MACIndex mapping for the preamble shall be as specified in Table  
 8 1.4.1.3.2.2-2.

9 The 64-chip preamble repetition factor shall be as specified in Table 1.4.1.3.2.3.1-1.

1

**Table 1.4.1.3.2.3.1-1. Preamble Repetition**

<b>Transmission Format (Physical Layer Packet Size (bits), Nominal Transmit Duration (slots), Preamble Length (chips))</b>	<b>64 chip Preamble Sequence Repetition</b>
(128, 16, 1024)	16
(128, 4, 1024)	16
(128, 8, 512)	8
(128, 4, 256)	4
(128, 2, 128)	2
(128, 1, 64)	1
(256, 16, 1024)	16
(256, 4, 1024)	16
(256, 8, 512)	8
(256, 4, 256)	4
(256, 2, 128)	2
(256, 1, 64)	1
(512, 16, 1024)	16
(512, 4, 1024)	16
(512, 8, 512)	8
(512, 4, 256)	4
(512, 4, 128)	2
(512, 2, 128)	2
(512, 2, 64)	1
(512, 1, 64)	1
(1024, 16, 1024)	16
(1024, 8, 512)	8
(1024, 4, 256)	4
(1024, 4, 128)	2
(1024, 2, 128)	2
(1024, 2, 64)	1
(1024, 1, 64)	1
(2048, 4, 128)	2
(2048, 2, 64)	1
(2048, 1, 64)	1

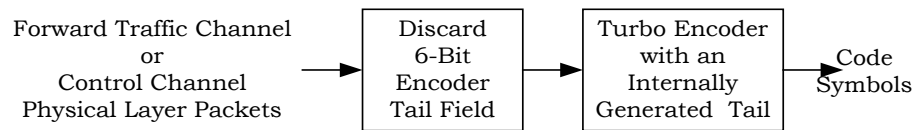
<b>Transmission Format (Physical Layer Packet Size (bits), Nominal Transmit Duration (slots), Preamble Length (chips))</b>	<b>64 chip Preamble Sequence Repetition</b>
(3072, 2, 64)	1
(3072, 1, 64)	1
(4096, 2, 64)	1
(4096, 1, 64)	1
(5120, 2, 64)	1
(5120, 1, 64)	1

1

## 2 1.4.1.3.2.3.2 Encoding

3 The Forward Traffic Channel physical layer packets and the Control Channel physical layer  
4 packets shall be encoded with code rates of  $R = 1/3$  or  $1/5$ . The encoder shall discard the  
5 6-bit TAIL field of the physical layer packet inputs and encode the remaining bits with a  
6 parallel turbo encoder, as specified in 1.4.1.3.2.3.2.1. The turbo encoder will add an  
7 internally generated tail of  $6/R$  output code symbols, so that the total number of output  
8 symbols is  $1/R$  times the number of bits in the input physical layer packet.

9 Figure 1.4.1.3.2.3.2-1 illustrates the forward link encoding approach. The forward link  
10 encoder parameters shall be as specified in Table 1.4.1.3.2.3.2-1.



11

12

**Figure 1.4.1.3.2.3.2-1. Forward Link Encoder**

1

**Table 1.4.1.3.2.3.2-1. Parameters of the Forward Link Encoder**

<b>Transmission Format (Physical Layer Packet Size (bits), Nominal Transmit Duration (slots), Preamble Length (chips))</b>	<b>Turbo Encoder Input Bits</b>	<b>Code Rate</b>	<b>Turbo Encoder Output Symbols</b>
(128, 16, 1024)	122	1/5	640
(128, 4, 1024)	122	1/5	640
(128, 8, 512)	122	1/5	640
(128, 4, 256)	122	1/5	640
(128, 2, 128)	122	1/5	640
(128, 1, 64)	122	1/5	640
(256, 16, 1024)	250	1/5	1,280
(256, 4, 1024)	250	1/5	1,280
(256, 8, 512)	250	1/5	1,280
(256, 4, 256)	250	1/5	1,280
(256, 2, 128)	250	1/5	1,280
(256, 1, 64)	250	1/5	1,280
(512, 16, 1024)	506	1/5	2,560
(512, 4, 1024)	506	1/5	2,560
(512, 8, 512)	506	1/5	2,560
(512, 4, 256)	506	1/5	2,560
(512, 4, 128)	506	1/5	2,560
(512, 2, 128)	506	1/5	2,560
(512, 2, 64)	506	1/5	2,560
(512, 1, 64)	506	1/5	2,560
(1024, 16, 1024)	1,018	1/5	5,120
(1024, 8, 512)	1,018	1/5	5,120
(1024, 4, 256)	1,018	1/5	5,120
(1024, 4, 128)	1,018	1/5	5,120
(1024, 2, 128)	1,018	1/5	5,120
(1024, 2, 64)	1,018	1/5	5,120
(1024, 1, 64)	1,018	1/3	3,072
(2048, 4, 128)	2,042	1/3	6,144
(2048, 2, 64)	2,042	1/3	6,144
(2048, 1, 64)	2,042	1/3	6,144

<b>Transmission Format (Physical Layer Packet Size (bits), Nominal Transmit Duration (slots), Preamble Length (chips))</b>	<b>Turbo Encoder Input Bits</b>	<b>Code Rate</b>	<b>Turbo Encoder Output Symbols</b>
(3072, 2, 64)	3,066	1/3	9,216
(3072, 1, 64)	3,066	1/3	9,216
(4096, 2, 64)	4,090	1/3	12,288
(4096, 1, 64)	4,090	1/3	12,288
(5120, 2, 64)	5,114	1/3	15,360
(5120, 1, 64)	5,114	1/3	15,360

1

## 2 1.4.1.3.2.3.2.1 Turbo Encoder

3 The turbo encoder employs two systematic, recursive, convolutional encoders connected in  
4 parallel, with an interleaver, the turbo interleaver, preceding the second recursive  
5 convolutional encoder. The two recursive convolutional codes are called the constituent  
6 codes of the turbo code. The outputs of the constituent encoders are punctured and  
7 repeated to achieve the desired number of turbo encoder output symbols.

8 The transfer function for the constituent code shall be

$$G(D) = \begin{bmatrix} 1 & \frac{n_0(D)}{d(D)} & \frac{n_1(D)}{d(D)} \end{bmatrix}$$

9

10 where  $d(D) = 1 + D^2 + D^3$ ,  $n_0(D) = 1 + D + D^3$ , and  $n_1(D) = 1 + D + D^2 + D^3$ .

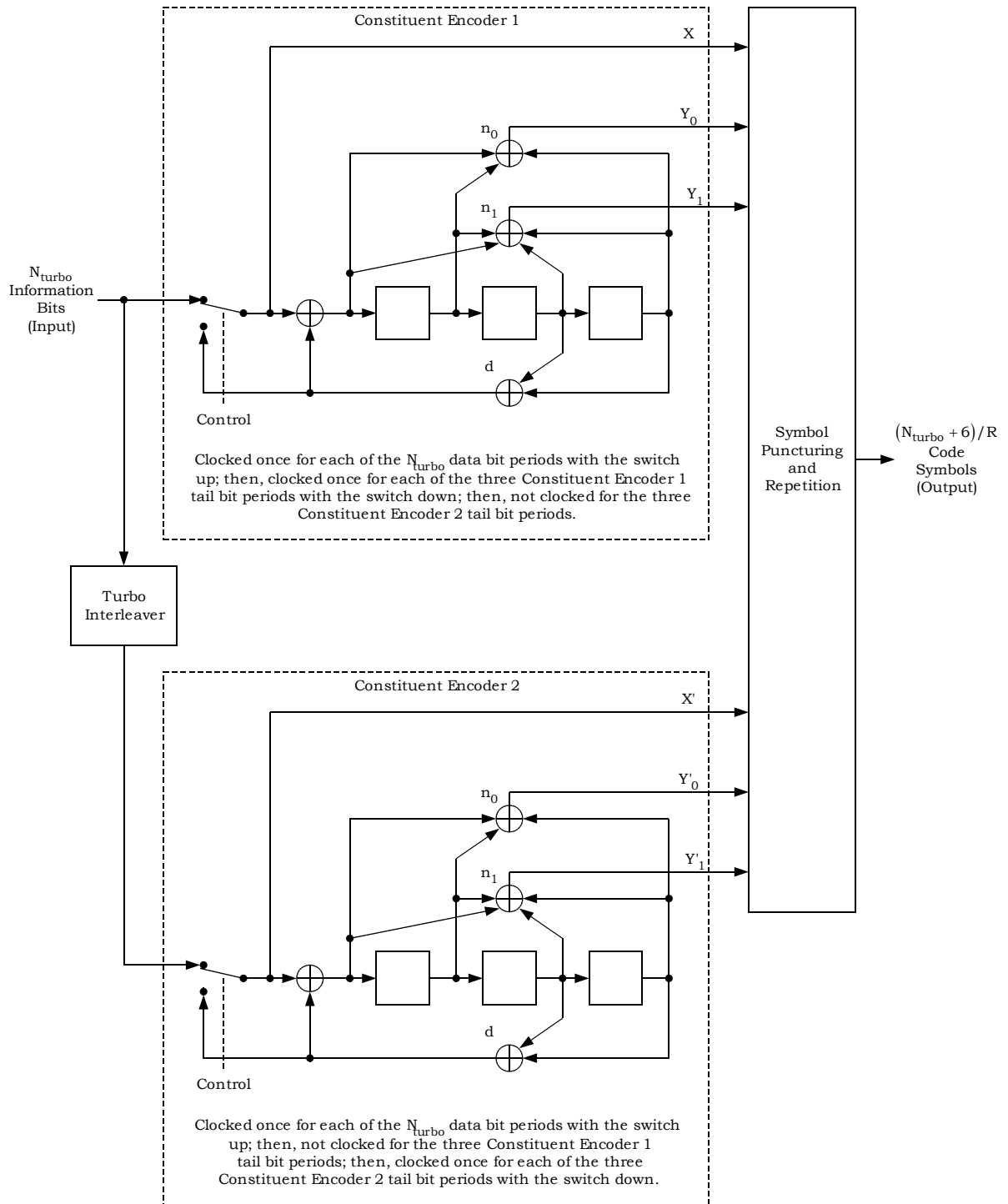
11 The turbo encoder shall generate an output symbol sequence that is identical to the one  
12 generated by the encoder shown in Figure 1.4.1.3.2.3.2.1-1. Initially, the states of the  
13 constituent encoder registers in this figure are set to zero. Then, the constituent encoders  
14 are clocked with the switches in the positions noted.

15 Let  $N_{\text{turbo}}$  be the number of bits into the turbo encoder after the 6-bit physical layer packet  
16 TAIL field is discarded. Then, the encoded data output symbols are generated by clocking  
17 the constituent encoders  $N_{\text{turbo}}$  times with the switches in the up positions and puncturing  
18 the outputs as specified in Table 1.4.1.3.2.3.2.1-1. Within a puncturing pattern, a '0'  
19 means that the symbol shall be deleted and a '1' means that the symbol shall be passed  
20 onwards. The constituent encoder outputs for each bit period shall be output in the  
21 sequence  $X, Y_0, Y_1, X', Y'_0, Y'_1$  with the  $X$  output first. Symbol repetition is not used in  
22 generating the encoded data output symbols.

23 The turbo encoder shall generate 6/R tail output symbols following the encoded data  
24 output symbols. This tail output symbol sequence shall be identical to the one generated by  
25 the encoder shown in Figure 1.4.1.3.2.3.2.1-1. The tail output symbols are generated after  
26 the constituent encoders have been clocked  $N_{\text{turbo}}$  times with the switches in the up  
27 position. The first 3/R tail output symbols are generated by clocking Constituent Encoder 1  
28 three times with its switch in the down position while Constituent Encoder 2 is not clocked

1 and puncturing and repeating the resulting constituent encoder output symbols. The last  
2 3/R tail output symbols are generated by clocking Constituent Encoder 2 three times with  
3 its switch in the down position while Constituent Encoder 1 is not clocked and puncturing  
4 and repeating the resulting constituent encoder output symbols. The constituent encoder  
5 outputs for each bit period shall be output in the sequence  $X, Y_0, Y_1, X', Y'_0, Y'_1$  with the  $X$   
6 output first.

7 The constituent encoder output symbol puncturing for the tail symbols shall be as specified  
8 in Table 1.4.1.3.2.3.2.1-2. Within a puncturing pattern, a '0' means that the symbol shall  
9 be deleted and a '1' means that the symbol shall be passed onwards. For rate 1/5 turbo  
10 codes, the tail output code symbols for each of the first three tail bit periods shall be  
11 punctured and repeated to achieve the sequence  $XXY_0Y_1Y_1$ , and the tail output code  
12 symbols for each of the last three tail bit periods shall be punctured and repeated to  
13 achieve the sequence  $X'X'Y'_0Y'_1Y'_1$ . For rate 1/3 turbo codes, the tail output symbols for  
14 each of the first three tail bit periods shall be  $XXY_0$ , and the tail output symbols for each of  
15 the last three tail bit periods shall be  $X'X'Y'_0$ .



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**Figure 1.4.1.3.2.3.2.1-1. Turbo Encoder**

1

**Table 1.4.1.3.2.3.2.1-1. Puncturing Patterns for the Data Bit Periods**

Output	Code Rate	
	1/3	1/5
X	1	1
Y <sub>0</sub>	1	1
Y <sub>1</sub>	0	1
X'	0	0
Y' <sub>0</sub>	1	1
Y' <sub>1</sub>	0	1

Note: For each rate, the puncturing table shall be read from top to bottom.

2

3

**Table 1.4.1.3.2.3.2.1-2. Puncturing Patterns for the Tail Bit Periods**

Output	Code Rate	
	1/3	1/5
X	111 000	111 000
Y <sub>0</sub>	111 000	111 000
Y <sub>1</sub>	000 000	111 000
X'	000 111	000 111
Y' <sub>0</sub>	000 111	000 111
Y' <sub>1</sub>	000 000	000 111

Note: For Rate 1/3 turbo codes, the puncturing table shall be read first from top to bottom repeating X and X', and then from left to right. For Rate 1/5 turbo codes, the puncturing table shall be read first from top to bottom repeating X, X', Y<sub>1</sub>, and Y'<sub>1</sub> and then from left to right.

4

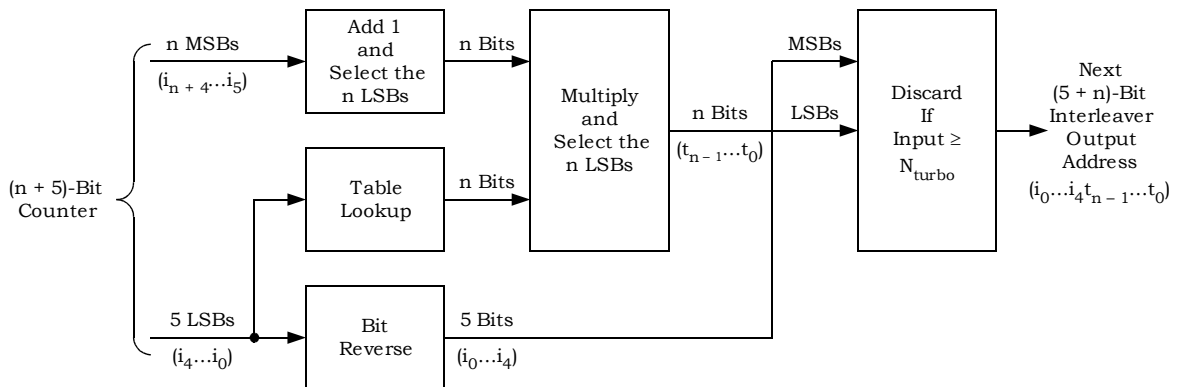
5 1.4.1.3.2.3.2.2 Turbo Interleaver

6 The turbo interleaver, which is part of the turbo encoder, shall block interleave the turbo  
7 encoder input data that is fed to Constituent Encoder 2.

8 The turbo interleaver shall be functionally equivalent to an approach where the entire  
9 sequence of turbo interleaver input bits are written sequentially into an array at a sequence  
10 of addresses, and then the entire sequence is read out from a sequence of addresses that  
11 are defined by the procedure described below.

1 Let the sequence of input addresses be from 0 to  $N_{turbo} - 1$ . Then, the sequence of  
 2 interleaver output addresses shall be equivalent to those generated by the procedure  
 3 illustrated in Figure 1.4.1.3.2.3.2.2-1 and described below.<sup>8</sup>

- 4 1. Determine the turbo interleaver parameter,  $n$ , where  $n$  is the smallest integer such  
 5 that  $N_{turbo} \leq 2^{n+5}$ . Table 1.4.1.3.2.3.2.2-1 gives this parameter for the different  
 6 physical layer packet sizes.
- 7 2. Initialize an  $(n + 5)$ -bit counter to 0.
- 8 3. Extract the  $n$  most significant bits (MSBs) from the counter and add one to form a  
 9 new value. Then, discard all except the  $n$  least significant bits (LSBs) of this value.
- 10 4. Obtain the  $n$ -bit output of the table lookup defined in Table 1.4.1.3.2.3.2.2-2 with a  
 11 read address equal to the five LSBs of the counter. Note that this table depends on  
 12 the value of  $n$ .
- 13 5. Multiply the values obtained in Steps 3 and 4, and discard all except the  $n$  LSBs.
- 14 6. Bit-reverse the five LSBs of the counter.
- 15 7. Form a tentative output address that has its MSBs equal to the value obtained in  
 16 Step 6 and its LSBs equal to the value obtained in Step 5.
- 17 8. Accept the tentative output address as an output address if it is less than  $N_{turbo}$ ;  
 18 otherwise, discard it.
- 19 9. Increment the counter and repeat Steps 3 through 8 until all  $N_{turbo}$  interleaver  
 20 output addresses are obtained.



21  
 22

**Figure 1.4.1.3.2.3.2.2-1. Turbo Interleaver Output Address Calculation Procedure**

<sup>8</sup> This procedure is equivalent to one where the counter values are written into a  $2^5$ -row by  $2^n$ -column array by rows, the rows are shuffled according to a bit-reversal rule, the elements within each row are permuted according to a row-specific linear congruential sequence, and tentative output addresses are read out by column. The linear congruential sequence rule is  $x(i + 1) = (x(i) + c) \bmod 2^n$ , where  $x(0) = c$  and  $c$  is a row-specific value from a table lookup.

1

**Table 1.4.1.3.2.3.2.2-1. Turbo Interleaver Parameter**

<b>Physical Layer Packet Size</b>	<b>Turbo Interleaver Block Size <math>N_{\text{turbo}}</math></b>	<b>Turbo Interleaver Parameter <b>n</b></b>
128	122	2
256	250	3
512	506	4
1,024	1,018	5
2,048	2,042	6
3,072	3,066	7
4,096	4,090	7
5,120	5,114	8

2

1

**Table 1.4.1.3.2.3.2.2-2. Turbo Interleaver Lookup Table Definition**

<b>Table Index</b>	<b>n = 2 Entries</b>	<b>n = 3 Entries</b>	<b>n = 4 Entries</b>	<b>n = 5 Entries</b>	<b>n = 6 Entries</b>	<b>n = 7 Entries</b>	<b>n = 8 Entries</b>
0	3	1	5	27	3	15	3
1	3	1	15	3	27	127	1
2	3	3	5	1	15	89	5
3	1	5	15	15	13	1	83
4	3	1	1	13	29	31	19
5	1	5	9	17	5	15	179
6	3	1	9	23	1	61	19
7	1	5	15	13	31	47	99
8	1	3	13	9	3	127	23
9	1	5	15	3	9	17	1
10	3	3	7	15	15	119	3
11	1	5	11	3	31	15	13
12	1	3	15	13	17	57	13
13	1	5	3	1	5	123	3
14	1	5	15	13	39	95	17
15	3	1	5	29	1	5	1
16	3	3	13	21	19	85	63
17	1	5	15	19	27	17	131
18	3	3	9	1	15	55	17
19	3	5	3	3	13	57	131
20	3	3	1	29	45	15	211
21	1	5	3	17	5	41	173
22	3	5	15	25	33	93	231
23	1	5	1	29	15	87	171
24	3	1	13	9	13	63	23
25	1	5	1	13	9	15	147
26	3	1	9	23	15	13	243
27	1	5	15	13	31	15	213
28	3	3	11	13	17	81	189
29	1	5	3	1	5	57	51
30	1	5	15	13	15	31	15
31	3	3	5	13	33	69	67

2

## 1 1.4.1.3.2.3.3 Scrambling

2 The output of the encoder shall be scrambled to randomize the data prior to modulation.  
3 The scrambling sequence shall be equivalent to one generated with a 17-tap linear feedback  
4 shift register with a generator sequence of  $h(D) = D^{17} + D^{14} + 1$ , as shown in Figure  
5 1.4.1.3.2.3.3-1. At the start of the physical layer packet, the shift register shall be  
6 initialized to the state  $[1 \ 1 \ 1 \ b_2 \ b_1 \ b_0 \ \overline{r_6} \ r_5 \ r_4 \ r_3 \ r_2 \ r_1 \ r_0 \ d_3 \ d_2 \ d_1 \ d_0]$ . The  $r_6 r_5 r_4 r_3 r_2 r_1 r_0$  bits shall be  
7 equal to the 7-bit preamble MACIndex value (see Table 1.4.1.3.2.2-2). The  $d_3 d_2 d_1 d_0$  bits  
8 shall be determined by the nominal data rate, as specified in Table 1.4.1.3.2.3.3-1. The  
9  $b_2 b_1 b_0$  bits shall be determined by the payload size, as specified in Table 1.4.1.3.2.3.3-1.  
10 The initial state shall generate the first scrambling bit. The shift register shall be clocked  
11 once for every encoder output code symbol to generate a bit of the scrambling sequence.  
12 Every encoder output code symbol shall be XOR'd with the corresponding bit of the  
13 scrambling sequence to yield a scrambled encoded bit.

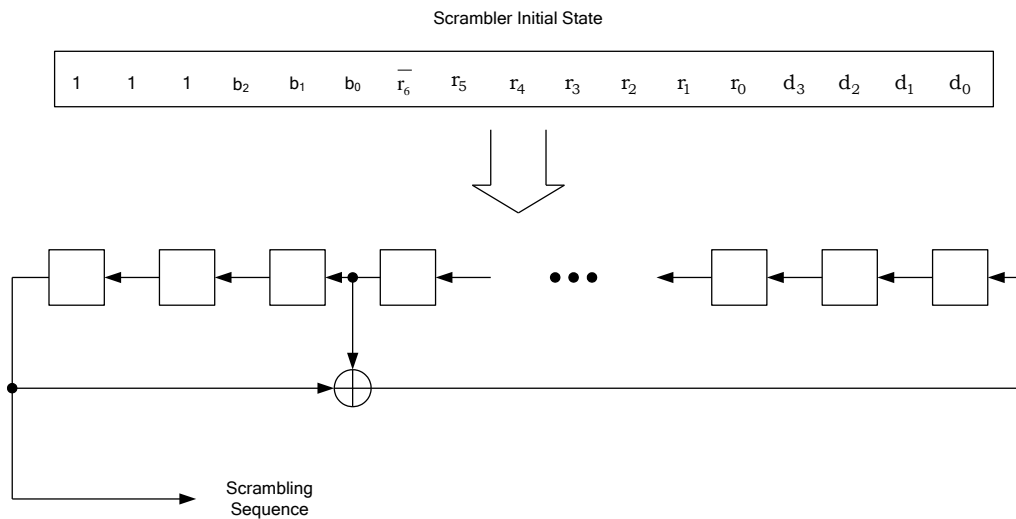
1

**Table 1.4.1.3.2.3.3-1. Parameters Controlling the Scrambler Initial State**

<b>Transmission Format (Physical Layer Packet Size (bits), Nominal Transmit Duration (slots), Preamble Length (chips))</b>	<b>b<sub>2</sub></b>	<b>b<sub>1</sub></b>	<b>b<sub>0</sub></b>	<b>d<sub>3</sub></b>	<b>d<sub>2</sub></b>	<b>d<sub>1</sub></b>	<b>d<sub>0</sub></b>	<b>Nominal Data Rate (kbps)</b>
(128, 16, 1024)	0	0	0	0	0	0	1	4.8
(128, 8, 512)	0	0	0	0	0	1	0	9.6
(128, 4, 256)	0	0	0	0	0	1	1	19.2
(128, 4, 1024)	0	0	0	0	0	1	1	19.2
(128, 2, 128)	0	0	0	0	1	0	0	38.4
(128, 1, 64)	0	0	0	0	1	1	0	76.8
(256, 16, 1024)	0	0	1	0	0	0	1	9.6
(256, 8, 512)	0	0	1	0	0	1	0	19.2
(256, 4, 256)	0	0	1	0	0	1	1	38.4
(256, 4, 1024)	0	0	1	0	0	1	1	38.4
(256, 2, 128)	0	0	1	0	1	0	0	76.8
(256, 1, 64)	0	0	1	0	1	1	0	153.6
(512, 16, 1024)	0	1	0	0	0	0	1	19.2
(512, 8, 512)	0	1	0	0	0	1	0	38.4
(512, 4, 256)	0	1	0	0	0	1	1	76.8
(512, 4, 1024)	0	1	0	0	0	1	1	76.8
(512, 4, 128)	0	1	0	0	1	0	1	76.8
(512, 2, 128)	0	1	0	0	1	0	0	153.6
(512, 2, 64)	0	1	0	0	1	1	1	153.6
(512, 1, 64)	0	1	0	0	1	1	0	307.2
(1024, 16, 1024)	1	1	1	0	0	0	1	38.4
(1024, 8, 512)	1	1	1	0	0	1	0	76.8
(1024, 4, 256)	1	1	1	0	0	1	1	153.6
(1024, 4, 128)	0	1	1	0	1	0	1	153.6
(1024, 2, 128)	1	1	1	0	1	0	0	307.2
(1024, 2, 64)	0	1	1	0	1	1	1	307.2
(1024, 1, 64)	1	1	1	0	1	1	0	614.4

<b>Transmission Format (Physical Layer Packet Size (bits), Nominal Transmit Duration (slots), Preamble Length (chips))</b>	<b>b<sub>2</sub></b>	<b>b<sub>1</sub></b>	<b>b<sub>0</sub></b>	<b>d<sub>3</sub></b>	<b>d<sub>2</sub></b>	<b>d<sub>1</sub></b>	<b>d<sub>0</sub></b>	<b>Nominal Data Rate (kbps)</b>
(2048, 4, 128)	1	1	1	0	1	0	1	307.2
(2048, 2, 64)	1	1	1	0	1	1	1	614.4
(2048, 1, 64)	1	1	1	1	0	0	1	1228.8
(3072, 2, 64)	1	1	1	1	0	0	0	921.6
(3072, 1, 64)	1	1	1	1	0	1	1	1843.2
(4096, 2, 64)	1	1	1	1	0	1	0	1228.8
(4096, 1, 64)	1	1	1	1	1	0	0	2457.6
(5120, 2, 64)	1	1	1	1	1	0	1	1536.0
(5120, 1, 64)	1	1	1	1	1	1	0	3072.0

1



2

3

**Figure 1.4.1.3.2.3.3-1. Symbol Scrambler**

4 1.4.1.3.2.3.4 Channel Interleaving

5 The sequence of binary symbols at the output of the encoder shall be interleaved with a  
 6 Channel Interleaver. Channel interleaving shall consist of a Symbol Reordering stage  
 7 followed by a Matrix Interleaving stage which is followed by a Short Sequence Repetition  
 8 Stage.

1 The packet length,  $N$  (including data and tail bits) is expressed as  $N = R \times K \times 2^m$ , where  $R$ ,  
 2  $K$  and  $m$  are positive integers. The channel interleaver is described in terms of the  
 3 parameters  $R$ ,  $K$ ,  $m$ , a short-packet wrap-around parameter  $W$ , and an end-around-shift  
 4 parameter  $D$ .

#### 5 1.4.1.3.2.3.4.1 Symbol Reordering

6 The scrambled turbo encoder data and tail output symbols generated with the rate 1/5  
 7 encoder shall be reordered according to the following procedure:

- 8 1. All of the scrambled data and tail turbo encoder output symbols shall be  
 9 demultiplexed into five sequences denoted  $U$ ,  $V0$ ,  $V1$ ,  $V'0$ , and  $V'1$ . The scrambled  
 10 encoder output symbols shall be sequentially distributed from the  $U$  sequence to the  
 11  $V'1$  sequence with the first scrambled encoder output symbol going to the  $U$   
 12 sequence, the second to the  $V0$  sequence, the third to the  $V1$  sequence, the fourth  
 13 to the  $V'0$  sequence, the fifth to the  $V'1$  sequence, the sixth to the  $U$  sequence, etc.
- 14 2. The  $U$ ,  $V0$ ,  $V1$ ,  $V'0$ , and  $V'1$  sequences shall be ordered according to  $UV0V'0V'1V'1$ .  
 15 That is, the  $U$  sequence of symbols shall be first and the  $V'1$  sequence of symbols  
 16 shall be last.

17 The scrambled turbo encoder data and tail output symbols generated with the rate 1/3  
 18 encoder shall be reordered according to the following procedure:

- 19 1. All of the scrambled data and tail turbo encoder output symbols shall be  
 20 demultiplexed into three sequences denoted  $U$ ,  $V0$  and  $V'0$ . The scrambled encoder  
 21 output symbols shall be sequentially distributed from the  $U$  sequence to the  $V'0$   
 22 sequence with the first scrambled encoder output symbol going to the  $U$  sequence,  
 23 the second to the  $V0$  sequence, the third to the  $V'0$  sequence, the fourth to the  $U$   
 24 sequence, etc.
- 25 2. The  $U$ ,  $V0$  and  $V'0$  sequences shall be ordered according to  $UV0V'0$ . That is, the  $U$   
 26 sequence of symbols shall be first and the  $V'0$  sequence of symbols shall be last.

#### 27 1.4.1.3.2.3.4.2 Matrix Interleaving

28 The Matrix Interleaving operation is carried out in the following steps:

- 29 1. The  $N$  symbols of the  $U$ -sequence symbols are written into a 3-dimensional cuboidal  
 30 array with  $R$  rows,  $C \equiv 2^m$  columns, and  $K$  levels. Symbols are written into the 3-  
 31 dimensional array with level-index incrementing first, followed by column-index,  
 32 followed by row-index. In other words, the  $i^{\text{th}}$  incoming symbol  $((r \times C + c) \times K + k)$ ,  
 33 where  $0 \leq i < N$  goes into the  $r^{\text{th}}$  row,  $c^{\text{th}}$  column, and  $k^{\text{th}}$  level where,  $0 \leq r < R$ ,  $0 \leq$   
 34  $c < C$ , and  $0 \leq k < K$ .
- 35 2. The linear array of  $R$  symbols, at the  $c^{\text{th}}$  column and  $k^{\text{th}}$  level, is end-around-shifted  
 36 by  $(c \times K + k) \bmod R$ . In other words, matrix[  $r$  ] [  $c$  ] [  $k$  ] is transformed to matrix[ $(r$   
 37  $+ c \times K + k) \bmod R$ ] [  $c$  ] [  $k$  ].
- 38 3. The linear array of  $C \equiv 2^m$  symbols, at each given level and row, is bit-reverse  
 39 interleaved (based on column-index).

- 1 4. If  $K > 3$ , then the symbols at level given by  $\lfloor K/2 \rfloor$  are swapped with symbols at level  
2 1 ( $k=1$ ).
- 3 5. Symbols from the cuboidal array are read out with row-index incrementing first,  
4 followed by column-index, followed by level-index. In other words, the  $i^{\text{th}}$  output  
5 symbol  $((k \times C + c) \times R + r)$ , where  $0 \leq i < N$  comes from the  $r^{\text{th}}$  row,  $c^{\text{th}}$  column, and  
6  $k^{\text{th}}$  level where,  $0 \leq r < R$ ,  $0 \leq c < C$ , and  $0 \leq k < K$ .
- 7 6. The  $N$  symbols of the  $V_0$  sequence, followed by the  $N$  symbols of the  $V_0'$  sequence  
8 are written into with  $R$  rows,  $C \equiv 2^{m+1}$  columns and  $K$  levels. Symbols are written  
9 into the 3-dimensional array with level-index incrementing first, followed by  
10 column-index, followed by row-index. In other words, the  $i^{\text{th}}$  incoming symbol  $((r \times C$   
11  $+ c) \times K + k)$ , where  $0 \leq i < 2 \times N$  goes into the  $r^{\text{th}}$  row,  $c^{\text{th}}$  column, and  $k^{\text{th}}$  level,  
12 where  $0 \leq r < R$ ,  $0 \leq c < C$ , and  $0 \leq k < K$ .
- 13 7. The linear array of  $R$  symbols, at the  $c^{\text{th}}$  column and  $k^{\text{th}}$  level, is end-around-  
14 shifted by the amount  $\lfloor (K \times c + k) / D \rfloor \bmod R$ . In other words,  $\text{matrix}[r][c][k]$  is  
15 transformed to  $\text{matrix}[r + \lfloor (K \times c + k) / D \rfloor \bmod R][c][k]$ .
- 16 8. The linear array of  $C \equiv 2^{m+1}$  symbols, at each given level and row, is bit-reverse  
17 interleaved (based on column-index).
- 18 9. If  $K > 3$ , then the symbols at level  $\lfloor K/2 \rfloor$  are swapped with symbols at level 1 ( $k=1$ ).
- 19 10. Symbols from the cuboidal array are read out with row-index incrementing first,  
20 followed by column-index, followed by level-index. In other words, the  $i^{\text{th}}$  output  
21 symbol  $((k \times C + c) \times R + r)$ , where  $0 \leq i < 2 \times N$  comes from the  $r^{\text{th}}$  row,  $c^{\text{th}}$  column  
22 and  $k^{\text{th}}$  level, where,  $0 \leq r < R$ ,  $0 \leq c < C$ , and  $0 \leq k < K$ .
- 23 11. The sequence of  $V_1$  and  $V_1'$  symbols are processed similar to the  $V_0$  and  $V_0'$   
24 symbols, as described in 5 through 8.

#### 25 1.4.1.3.2.3.4.3 Short Sequence Repetition

26 If the total number of symbols ( $3 \times N$  or  $5 \times N$ ) output by the Matrix Interleaving stage as  
27 described above is less than the wrap-around parameter  $W$ , then the output sequence is  
28 repeated partially or fully so that the length of the sequence is equal to  $W$  binary symbols.  
29 Otherwise, the symbol sequence output by the matrix interleaver described above is  
30 regarded as the output of the channel interleaver. Table 1.4.1.3.2.3.4.3-1 below shows the  
31 interleaver parameters for various packets used on the Forward Traffic Channel.

1

**Table 1.4.1.3.2.3.4.3-1. Channel Interleaver Parameters**

<b>Transmission Format (Physical Layer Packet Size (bits), Nominal Transmit Duration (slots), Preamble Length (chips))</b>	<b>N</b>	<b>K</b>	<b>R</b>	<b>m</b>	<b>D</b>	<b>W</b>
(128, 16, 1024)	128	1	2	6	4	0
(128, 8, 512)	128	1	2	6	4	0
(128, 4, 1024)	128	1	2	6	4	0
(128, 4, 256)	128	1	2	6	4	0
(128, 2, 128)	128	1	2	6	4	0
(128, 1, 64)	128	1	2	6	4	0
(256, 16, 1024)	256	1	2	7	4	0
(256, 8, 512)	256	1	2	7	4	0
(256, 4, 1024)	256	1	2	7	4	0
(256, 4, 256)	256	1	2	7	4	0
(256, 2, 128)	256	1	2	7	4	0
(256, 1, 64)	256	1	2	7	4	0
(512, 16, 1024)	512	1	2	8	4	0
(512, 8, 512)	512	1	2	8	4	0
(512, 4, 1024)	512	1	2	8	4	0
(512, 4, 256)	512	1	2	8	4	0
(512, 4, 128)	512	1	2	8	4	6,144
(512, 2, 128)	512	1	2	8	4	0
(512, 2, 64)	512	1	2	8	4	6,144
(512, 1, 64)	512	1	2	8	4	0
(1024, 16, 1024)	1024	1	2	9	4	0
(1024, 8, 512)	1024	1	2	9	4	0
(1024, 4, 256)	1024	1	2	9	4	0
(1024, 4, 128)	1024	1	2	9	4	6,144
(1024, 2, 128)	1024	1	2	9	4	0
(1024, 2, 64)	1024	1	2	9	4	6,144
(1024, 1, 64)	1024	1	2	9	4	0
(2048, 4, 128)	2048	1	2	10	4	0
(2048, 2, 64)	2048	1	2	10	4	0

<b>Transmission Format (Physical Layer Packet Size (bits), Nominal Transmit Duration (slots), Preamble Length (chips))</b>	<b>N</b>	<b>K</b>	<b>R</b>	<b>m</b>	<b>D</b>	<b>W</b>
(2048, 1, 64)	2048	1	2	10	4	0
(3072, 2, 64)	3072	1	3	10	4	0
(3072, 1, 64)	3072	1	3	10	4	0
(4096, 2, 64)	4096	1	4	10	4	0
(4096, 1, 64)	4096	1	4	10	4	0
(5120, 2, 64)	5120	5	4	8	10	0
(5120, 1, 64)	5120	5	4	8	10	0

1

## 2 1.4.1.3.2.3.5 Modulation

3 The output of the channel interleaver shall be applied to a modulator that outputs an in-  
4 phase stream and a quadrature stream of modulated values. The modulator generates  
5 QPSK, 8-PSK, or 16-QAM modulation symbols, depending on the data rate.

## 6 1.4.1.3.2.3.5.1 QPSK Modulation

7 For physical layer packet sizes of 128, 256, 512, 1,024, or 2,048 bits, two successive  
8 channel interleaver output symbols shall be grouped to form QPSK modulation symbols.  
9 Each group of two adjacent block interleaver output symbols,  $x(2k)$  and  $x(2k + 1)$ ,  $k = 0, \dots,$   
10  $M - 1$  shall be mapped into a complex modulation symbol  $(m_I(k), m_Q(k))$  as specified in  
11 Table 1.4.1.3.2.3.5.1-1. Figure 1.4.1.3.2.3.5.1-1 shows the signal constellation of the QPSK  
12 modulator, where  $s_0 = x(2k)$  and  $s_1 = x(2k + 1)$ .

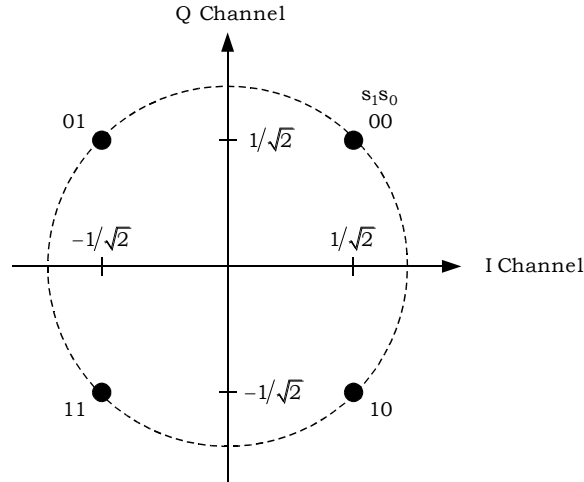
13

**Table 1.4.1.3.2.3.5.1-1. QPSK Modulation Table**

<b>Interleaved Symbols</b>		<b>Modulation Symbols</b>	
<b><math>s_1</math> <math>x(2k + 1)</math></b>	<b><math>s_0</math> <math>x(2k)</math></b>	<b><math>m_I(k)</math></b>	<b><math>m_Q(k)</math></b>
0	0	D	D
0	1	-D	D
1	0	D	-D
1	1	-D	-D

Note:  $D = 1/\sqrt{2}$ .

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**Figure 1.4.1.3.2.3.5.1-1. Signal Constellation for QPSK Modulation**

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1.4.1.3.2.3.5.2 8-PSK Modulation

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For physical layer packet sizes of 3,072 bits, three successive channel interleaver output symbols shall be grouped to form 8-PSK modulation symbols. Each group of three adjacent block interleaver output symbols,  $x(3k)$ ,  $x(3k + 1)$ , and  $x(3k + 2)$ ,  $k = 0, \dots, M - 1$  shall be mapped into a complex modulation symbol ( $m_I(k)$ ,  $m_Q(k)$ ) as specified in Table 1.4.1.3.2.3.5.2-1. Figure 1.4.1.3.2.3.5.2-1 shows the signal constellation of the 8-PSK modulator, where  $s_0 = x(3k)$ ,  $s_1 = x(3k + 1)$ , and  $s_2 = x(3k + 2)$ .

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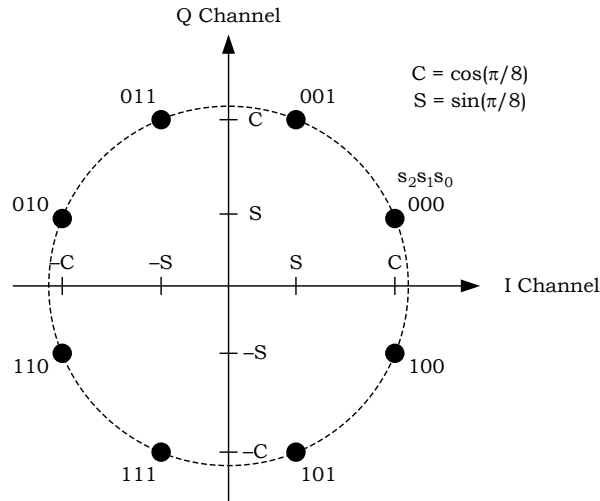
**Table 1.4.1.3.2.3.5.2-1. 8-PSK Modulation Table**

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Interleaved Symbols			Modulation Symbols	
$s_2$ $x(3k + 2)$	$s_1$ $x(3k + 1)$	$s_0$ $x(3k)$	$m_I(k)$	$m_Q(k)$
0	0	0	C	S
0	0	1	S	C
0	1	1	-S	C
0	1	0	-C	S
1	1	0	-C	-S
1	1	1	-S	-C
1	0	1	S	-C
1	0	0	C	-S

Note:  $C = \cos(\pi/8) \approx 0.9239$  and  $S = \sin(\pi/8) \approx 0.3827$ .

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**Figure 1.4.1.3.2.3.5.2-1. Signal Constellation for 8-PSK Modulation**

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1.4.1.3.2.3.5.3 16-QAM Modulation

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For physical layer packet sizes of 4,096 and 5,120 bits, four successive channel interleaver output symbols shall be grouped to form 16-QAM modulation symbols. Each group of four

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adjacent block interleaver output symbols,  $x(4k)$ ,  $x(4k + 1)$ ,  $x(4k + 2)$ , and  $x(4k + 3)$ ,  $k = 0, \dots, M - 1$  shall be mapped into a complex modulation symbol ( $m_I(k)$ ,  $m_Q(k)$ ) as specified in

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Table 1.4.1.3.2.3.5.3-1. Figure 1.4.1.3.2.3.5.3-1 shows the signal constellation of the 16-QAM modulator, where  $s_0 = x(4k)$ ,  $s_1 = x(4k + 1)$ ,  $s_2 = x(4k + 2)$ , and  $s_3 = x(4k + 3)$ .

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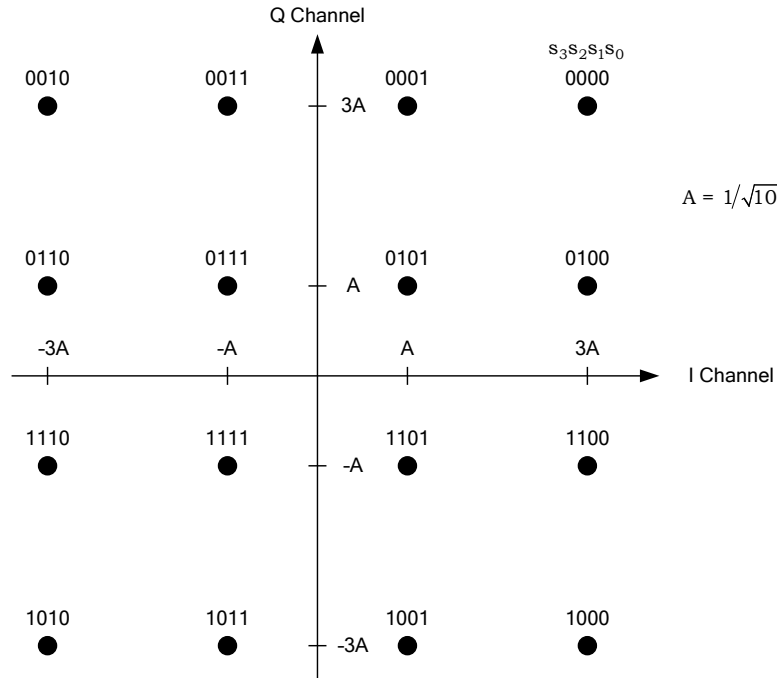
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**Table 1.4.1.3.2.3.5.3-1. 16-QAM Modulation Table**

Interleaved Symbols				Modulation Symbols	
$s_3$ $x(4k + 3)$	$s_2$ $x(4k + 2)$	$s_1$ $x(4k + 1)$	$s_0$ $x(4k)$	$m_Q(k)$	$m_I(k)$
0	0	0	0	3A	3A
0	0	0	1	3A	A
0	0	1	1	3A	-A
0	0	1	0	3A	-3A
0	1	0	0	A	3A
0	1	0	1	A	A
0	1	1	1	A	-A
0	1	1	0	A	-3A
1	1	0	0	-A	3A
1	1	0	1	-A	A
1	1	1	1	-A	-A
1	1	1	0	-A	-3A
1	0	0	0	-3A	3A
1	0	0	1	-3A	A
1	0	1	1	-3A	-A
1	0	1	0	-3A	-3A

Note:  $A = 1/\sqrt{10} \approx 0.3162$ .



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**Figure 1.4.1.3.2.3.5.3-1. Signal Constellation for 16-QAM Modulation**

1.4.1.3.2.3.6 Sequence Repetition and Symbol Puncturing

Table 1.4.1.3.2.3.6-1 gives the number of modulation symbols that the modulator provides per physical layer packet and the number of modulation symbols needed for the data portion of the allocated slots. If the number of required modulation symbols is more than the number provided, the complete sequence of input modulation symbols shall be repeated as many full-sequence times as possible followed by a partial transmission if necessary. If a partial transmission is needed, the first portion of the input modulation symbol sequence shall be used. If the number of required modulation symbols is less than the number provided, only the first portion of the input modulation symbol sequence shall be used.

The sequence repetition and symbol puncturing parameters shall be as specified in Table 1.4.1.3.2.3.6-1.

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**Table 1.4.1.3.2.3.6-1. Sequence Repetition and Symbol Puncturing Parameters**

<b>Transmission Format (Physical Layer Packet Size (bits), Nominal Transmit Duration (slots), Preamble Length (chips))</b>	<b>Values per Physical Layer Packet</b>				<b>Coding</b>	
	<b>Number of Modulation Symbols Provided</b>	<b>Number of Modulation Symbols Needed</b>	<b>Number of Full Sequence Transmissions</b>	<b>Number of Modulation Symbols in Last Partial Transmission</b>	<b>Effective Code Rate</b>	<b>Repetition Factor</b>
(128, 16, 1024)	320	24,576	76	256	1/5	76.8
(128, 8, 512)	320	12,288	38	128	1/5	38.4
(128, 4, 1024)	320	5,376	16	256	1/5	16.8
(128, 4, 256)	320	6,144	19	64	1/5	19.2
(128, 2, 128)	320	3,072	9	192	1/5	9.6
(128, 1, 64)	320	1,536	4	256	1/5	4.8
(256, 16, 1024)	640	24,576	38	256	1/5	38.4
(256, 8, 512)	640	12,288	19	128	1/5	19.2
(256, 4, 1024)	640	5,376	8	256	1/5	8.4
(256, 4, 256)	640	6,144	9	384	1/5	9.6
(256, 2, 128)	640	3,072	4	512	1/5	4.8
(256, 1, 64)	640	1,536	2	256	1/5	2.4
(512, 16, 1024)	1,280	24,576	19	256	1/5	19.2
(512, 8, 512)	1,280	12,288	9	768	1/5	9.6
(512, 4, 1024)	1,280	5,376	4	256	1/5	4.2
(512, 4, 256)	1,280	6,144	4	1,024	1/5	4.8
(512, 4, 128)	3,072	6,272	2	128	1/5	2.04
(512, 2, 128)	1,280	3,072	2	512	1/5	2.4
(512, 2, 64)	3,072	3,136	1	64	1/5	1.02
(512, 1, 64)	1,280	1,536	1	256	1/5	1.2
(1024, 16, 1024)	2,560	24,576	9	1,536	1/5	9.6
(1024, 8, 512)	2,560	12,288	4	2,048	1/5	4.8
(1024, 4, 256)	2,560	6,144	2	1,024	1/5	2.4
(1024, 4, 128)	3,072	6,272	2	128	1/5	2.04
(1024, 2, 128)	2,560	3,072	1	512	1/5	1.2
(1024, 2, 64)	3,072	3,136	1	64	1/5	1.02

<b>Transmission Format (Physical Layer Packet Size (bits), Nominal Transmit Duration (slots), Preamble Length (chips))</b>	<b>Values per Physical Layer Packet</b>				<b>Coding</b>	
	<b>Number of Modulation Symbols Provided</b>	<b>Number of Modulation Symbols Needed</b>	<b>Number of Full Sequence Transmissions</b>	<b>Number of Modulation Symbols in Last Partial Transmission</b>	<b>Effective Code Rate</b>	<b>Repetition Factor</b>
(1024, 1, 64)	1,536	1,536	1	0	1/3	1
(2048, 4, 128)	3,072	6,272	2	128	1/3	2.04
(2048, 2, 64)	3,072	3,136	1	64	1/3	1.02
(2048, 1, 64)	3,072	1,536	0	1,536	2/3	1
(3072, 2, 64)	3,072	3,136	1	64	1/3	1.02
(3072, 1, 64)	3,072	1,536	0	1,536	2/3	1
(4096, 2, 64)	3,072	3,136	1	64	1/3	1.02
(4096, 1, 64)	3,072	1,536	0	1,536	2/3	1
(5120, 2, 64)	3,840	3,136	0	3,136	20/49	1
(5120, 1, 64)	3,840	1,536	0	1,536	5/6	1

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## 2 1.4.1.3.2.3.7 Symbol Demultiplexing

3 The in-phase stream at the output of the sequence repetition operation shall be  
4 demultiplexed into 16 parallel streams labeled  $I_0, I_1, I_2, \dots, I_{15}$ . If  $m_I(0), m_I(1), m_I(2), m_I(3),$   
5 ... denotes the sequence of sequence-repeated modulation output values in the in-phase  
6 stream, then for each  $k = 0, 1, 2, \dots, 15$ , the  $k^{\text{th}}$  demultiplexed stream  $I_k$  shall consist of the  
7 values  $m_I(k), m_I(16 + k), m_I(32 + k), m_I(48 + k), \dots$

8 Similarly, the quadrature stream at the output of the sequence repetition operation shall be  
9 demultiplexed into 16 parallel streams labeled  $Q_0, Q_1, Q_2, \dots, Q_{15}$ . If  $m_Q(0), m_Q(1), m_Q(2),$   
10  $m_Q(3), \dots$  denotes the sequence of sequence-repeated modulation output values in the  
11 quadrature stream, then for each  $k = 0, 1, 2, \dots, 15$ , the  $k^{\text{th}}$  demultiplexed stream  $Q_k$  shall  
12 consist of the values  $m_Q(k), m_Q(16 + k), m_Q(32 + k), m_Q(48 + k), \dots$

13 Each demultiplexed stream at the output of the symbol demultiplexer shall consist of  
14 modulation values at the rate of 76.8 ksp/s.

## 15 1.4.1.3.2.3.8 Walsh Channel Assignment

16 The individual streams generated by the symbol demultiplexer shall be assigned to one of  
17 16 distinct Walsh channels. For each  $k = 0, 1, 2, \dots, 15$ , the demultiplexed streams with  
18 labels  $I_k$  and  $Q_k$  shall be assigned to the in-phase and quadrature phases, respectively, of  
19 the  $k^{\text{th}}$  Walsh channel  $W_k^{16}$ . The modulation values associated with the in-phase and

1 quadrature phase components of the same Walsh channel are referred to as Walsh  
2 symbols.

#### 3 1.4.1.3.2.3.9 Walsh Channel Scaling

4 The modulated symbols on each branch of each Walsh channel shall be scaled to maintain  
5 a constant total transmit power independent of data rate. For this purpose, each orthogonal  
6 channel shall be scaled by a gain of  $\frac{1}{\sqrt{16}} = \frac{1}{4}$ . The gain settings are normalized to a unity  
7 reference equivalent to unmodulated BPSK transmitted at full power.

#### 8 1.4.1.3.2.3.10 Walsh Chip Level Summing

9 The scaled Walsh chips associated with the 16 Walsh channels shall be summed on a chip-  
10 by-chip basis.

#### 11 1.4.1.3.2.4 Control Channel

12 The Control Channel transmits broadcast messages and access-terminal-directed  
13 messages. Control Channel packets belonging to the synchronous capsule shall be  
14 transmitted using a Transmission Format of (1024, 8, 512) corresponding to a data rate of  
15 76.8 kbps or using a Transmission Format of (1024, 16, 1024) corresponding to a data rate  
16 of 38.4 kbps. Control Channel packets belonging to an asynchronous or a sub-  
17 synchronous capsule shall be transmitted using Transmission Formats of (1024, 8, 512),  
18 (1024, 16, 1024), (128, 4, 1024), (256, 4, 1024), or (512, 4, 1024). The modulation  
19 characteristics shall be the same as those of the Forward Traffic Channel at the  
20 corresponding Transmission Format. The Control Channel transmissions shall be  
21 distinguished from Forward Traffic Channel transmissions by having a preamble that is  
22 covered by a bi-orthogonal cover sequence with MACIndex 2, 3, 71, or that specified by the  
23 CCShortPacketsMACIndex attribute as specified in 1.4.1.3.2.3.1. A MACIndex value of 2  
24 shall be used for the Transmission Format of (1024, 8, 512) or 76.8 kbps data rate, a  
25 MACIndex value of 3 shall be used for the Transmission Format of (1024, 16, 1024) or 38.4  
26 kbps data rate, and a MACIndex value of 71 or a MACIndex value specified by  
27 CCShortPacketsMACIndex attribute value shall be used for the Transmission Formats of  
28 (128, 4, 1024), (256, 4, 1024), or (512, 4, 1024).

#### 29 1.4.1.3.3 Time-Division Multiplexing

30 The Forward Traffic Channel or Control Channel data modulation chips shall be time-  
31 division multiplexed with the preamble, Pilot Channel, and MAC Channel chips according  
32 to the timing diagrams in Figure 1.4.1.3.3-1, Figure 1.4.1.3.3-2,

33 Figure 1.4.1.3.3-3, Figure 1.4.1.3.3-4 and Figure 1.4.1.3.3-5. The multiplexing parameters  
34 shall be as specified in Table 1.4.1.3.3-1 through Table 1.4.1.3.3-5.

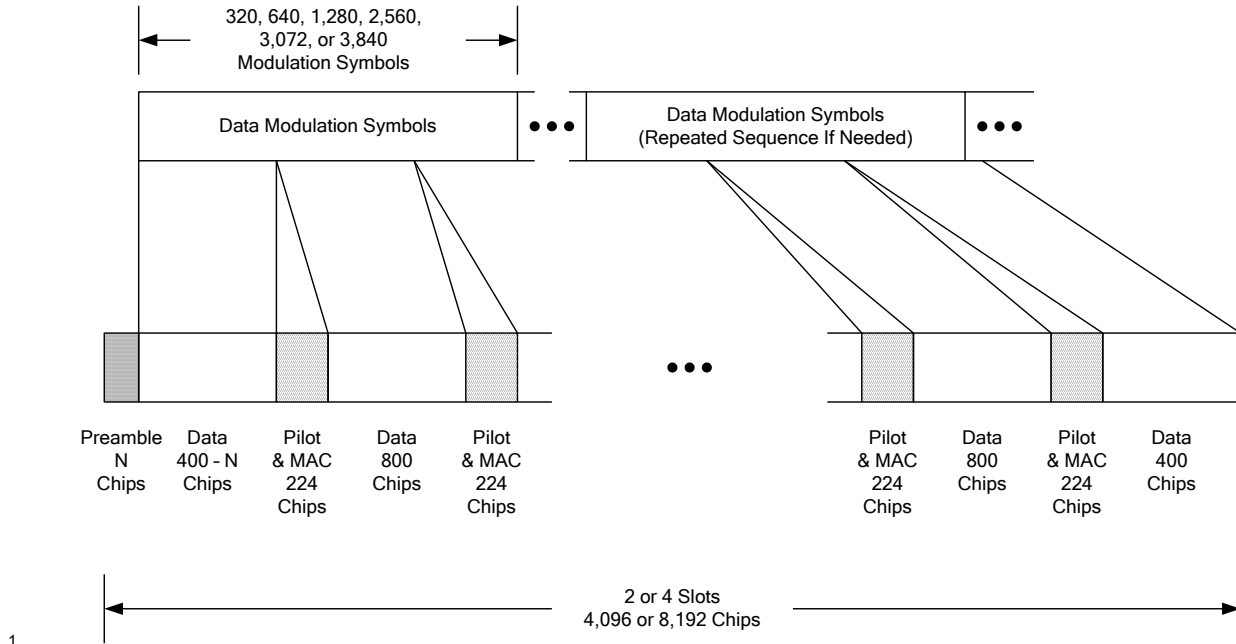
35 The Walsh chip rate shall be fixed at 1.2288 Mcps.

36 Forward Traffic Channel physical layer packets with Transmission Formats as shown in  
37 Table 1.4.1.3.3-1 shall be time division multiplexed with the preamble, Pilot Channel and  
38 MAC Channel chips according to the timing diagrams in Figure 1.4.1.3.3-1.

1 **Table 1.4.1.3.3-1. Transmission Formats Corresponding to Timing Diagram in Figure**  
 2 **1.4.1.3.3-1**

<b>Transmission Format (Physical Layer Packet Size (bits), Nominal Transmit Duration (slots), Preamble Length (chips))</b>
(128, 4, 256)
(128, 2, 128)
(256, 4, 256)
(256, 2, 128)
(512, 4, 256)
(512, 4, 128)
(512, 2, 128)
(512, 2, 64)
(1024, 4, 256)
(1024, 4, 128)
(1024, 2, 128)
(1024, 2, 64)
(2048, 4, 128)
(2048, 2, 64)
(3072, 2, 64)
(4096, 2, 64)
(5120, 2, 64)

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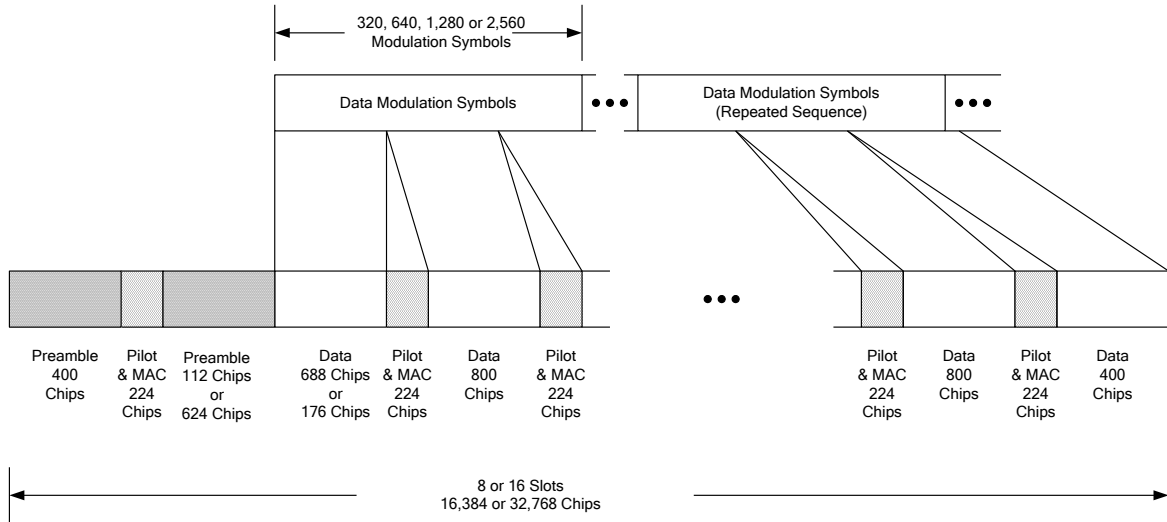
**Figure 1.4.1.3.3-1. Preamble, Pilot, MAC, and Data Multiplexing for the Multiple-Slot Cases with Transmission Formats in Table 1.4.1.3.3-1**

Forward Traffic Channel physical layer packets with Transmission Formats as shown in Table 1.4.1.3.3-2 shall be time division multiplexed with the preamble, Pilot Channel and MAC Channel chips according to the timing diagrams in Figure 1.4.1.3.3-2

**Table 1.4.1.3.3-2. Transmission Formats Corresponding to Timing Diagram in Figure 1.4.1.3.3-2**

<b>Transmission Format (Physical Layer Packet Size (bits), Nominal Transmit Duration (slots), Preamble Length (chips))</b>
(128, 16, 1024)
(128, 8, 512)
(256, 16, 1024)
(256, 8, 512)
(512, 16, 1024)
(512, 8, 512)
(1024, 16, 1024)
(1024, 8, 512)

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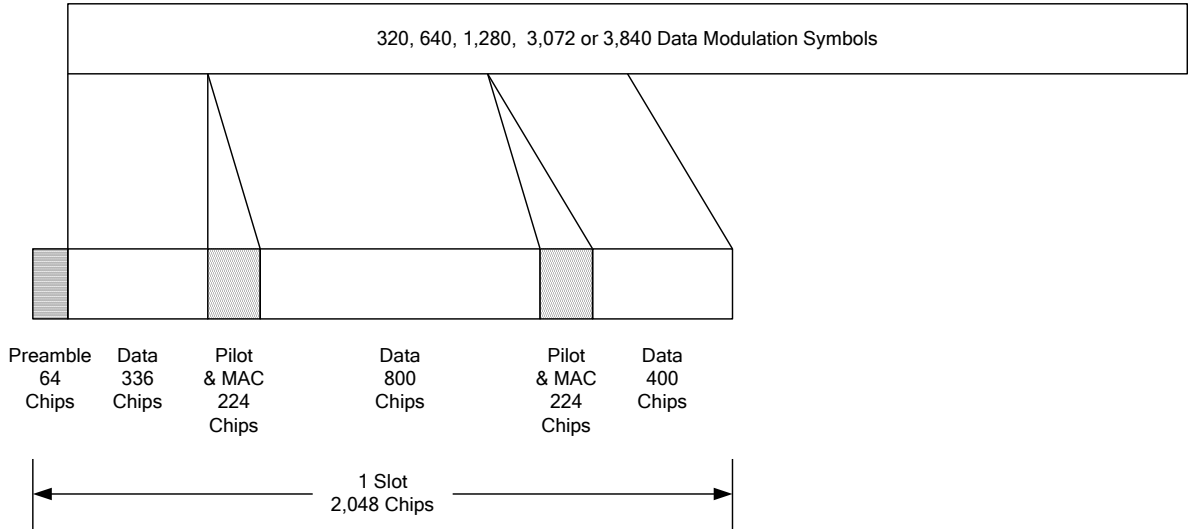


**Figure 1.4.1.3.3-2. Preamble, Pilot, MAC, and Data Multiplexing with Transmission Formats in Table 1.4.1.3.3-2**

Forward Traffic Channel physical layer packets with Transmission Formats as shown in Table 1.4.1.3.3-3 shall be time division multiplexed with the preamble, Pilot Channel and MAC Channel chips according to the timing diagrams in Figure 1.4.1.3.3-1.

**Table 1.4.1.3.3-3. Transmission Formats Corresponding to Timing Diagram in Figure 1.4.1.3.3-3**

<b>Transmission Format (Physical Layer Packet Size (bits), Nominal Transmit Duration (slots), Preamble Length (chips))</b>
(128, 1, 64)
(256, 1, 64)
(512, 1, 64)
(2048, 1, 64)
(3072, 1, 64)
(4096, 1, 64)
(5120, 1, 64)



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**Figure 1.4.1.3.3-3. Preamble, Pilot, MAC, and Data Multiplexing for the 1-Slot Cases with Transmission Formats in Table 1.4.1.3.3-3**

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Forward Traffic Channel physical layer packets with Transmission Formats as shown in Table 1.4.1.3.3-4 shall be time division multiplexed with the preamble, Pilot Channel and MAC Channel chips according to the timing diagrams in Figure 1.4.1.3.3-4.

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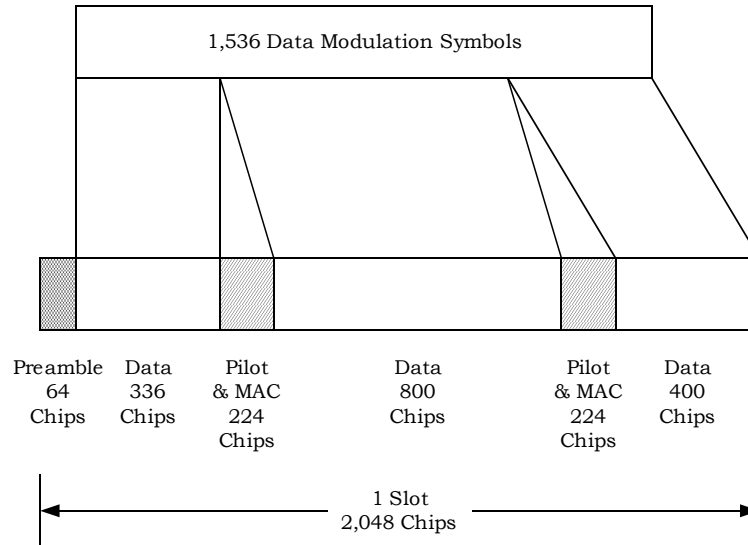
**Table 1.4.1.3.3-4. Transmission Formats Corresponding to Timing Diagram in Figure 1.4.1.3.3-4**

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Transmission Format (Physical Layer Packet Size (bits), Nominal Transmit Duration (slots), Preamble Length (chips))
(1024, 1, 64)

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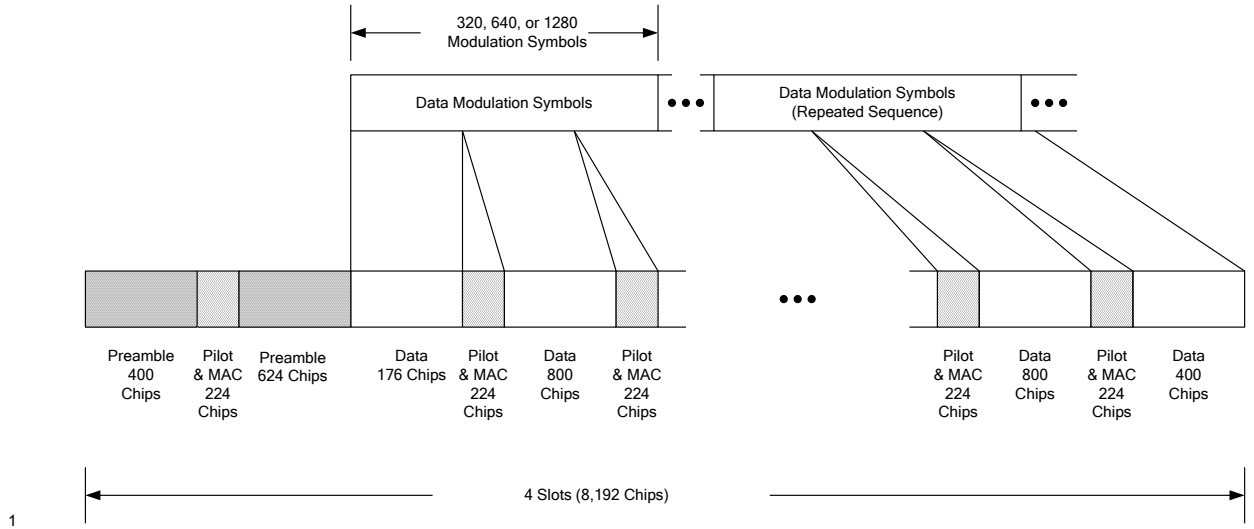
**Figure 1.4.1.3.3-4. Preamble, Pilot, MAC, and Data Multiplexing for the 1-Slot Case with Transmission Formats in Table 1.4.1.3.3-4.**

Forward Traffic Channel physical layer packets with Packet Transmission Formats as shown in Table 1.4.1.3.3-5 shall be time division multiplexed with the preamble, Pilot Channel and MAC Channel chips according to the timing diagrams in Figure 1.4.1.3.3-5.

**Table 1.4.1.3.3-5. Transmission Formats Corresponding to Timing Diagram in Figure 1.4.1.3.3-5**

<b>Transmission Format (Physical Layer Packet Size (bits), Nominal Transmit Duration (slots), Preamble Length (chips))</b>
(128, 4, 1,024)
(256, 4, 1,024)
(512, 4, 1,024)

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**Figure 1.4.1.3.3-5. Preamble, Pilot, MAC, and Data Multiplexing for the Multiple-Slot Cases with Transmission Formats in Table 1.4.1.3.3-5**

Table 1.4.1.3.3-6 shows the number of Pilot chips, MAC chips, and Data chips corresponding to each of the possible transmission formats.

1

**Table 1.4.1.3.3-6. Preamble, Pilot, MAC, and Data Multiplexing Parameters**

<b>Transmission Format (Physical Layer Packet Size (bits), Nominal Transmit Duration (slots), Preamble Length (chips))</b>	<b>Pilot chips</b>	<b>MAC chips</b>	<b>Data chips</b>
(128, 16, 1,024)	3,072	4,096	24,576
(128, 8, 512)	1,536	2,048	12,288
(128, 4, 1024)	768	1,024	5,376
(128, 4, 256)	768	1,024	6,144
(128, 2, 128)	384	512	3,072
(128, 1, 64)	192	256	1,536
(256, 16, 1024)	3,072	4,096	24,576
(256, 8, 512)	1,536	2,048	12,288
(256, 4, 1024)	768	1,024	5,376
(256, 4, 256)	768	1,024	6,144
(256, 2, 128)	384	512	3,072
(256, 1, 64)	192	256	1,536
(512, 16, 1024)	3,072	4,096	24,576
(512, 8, 512)	1,536	2,048	12,288
(512, 4, 1024)	768	1,024	5,376
(512, 4, 256)	768	1,024	6,144
(512, 4, 128)	768	1,024	6,272
(512, 2, 128)	384	512	3,072
(512, 2, 64)	384	512	3,136
(512, 1, 64)	192	256	1,536
(1024, 16, 1024)	3,072	4,096	24,576
(1024, 8, 512)	1,536	2,048	12,288
(1024, 4, 256)	768	1,024	6,144
(1024, 4, 128)	768	1,024	6,272
(1024, 2, 128)	384	512	3,072
(1024, 2, 64)	384	512	3,136
(1024, 1, 64)	192	256	1,536
(2048, 4, 128)	768	1,024	6,272
(2048, 2, 64)	384	512	3,136
(2048, 1, 64)	192	256	1,536

<b>Transmission Format (Physical Layer Packet Size (bits), Nominal Transmit Duration (slots), Preamble Length (chips))</b>	<b>Pilot chips</b>	<b>MAC chips</b>	<b>Data chips</b>
(3072, 2, 64)	384	512	3,136
(3072, 1, 64)	192	256	1,536
(4096, 2, 64)	384	512	3,136
(4096, 1, 64)	192	256	1,536
(5120, 2, 64)	384	512	3,136
(5120, 1, 64)	192	256	1,536

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## 2 1.4.1.3.4 Quadrature Spreading

3 Following orthogonal spreading, the combined modulation sequence shall be quadrature  
4 spread as shown in Figure 1.4.1.3.1-1. The spreading sequence shall be a quadrature  
5 sequence of length  $2^{15}$  (i.e., 32768 PN chips in length). This sequence is called the pilot PN  
6 sequence and shall be based on the following characteristic polynomials:

7 
$$P_I(x) = x^{15} + x^{10} + x^8 + x^7 + x^6 + x^2 + 1$$

8 (for the in-phase (I) sequence)

9 and

10 
$$P_Q(x) = x^{15} + x^{12} + x^{11} + x^{10} + x^9 + x^5 + x^4 + x^3 + 1$$

11 (for the quadrature-phase (Q) sequence).

12 The maximum length linear feedback shift-register sequences  $\{I(n)\}$  and  $\{Q(n)\}$  based on the  
13 above polynomials are of length  $2^{15} - 1$  and can be generated by the following linear  
14 recursions:

15 
$$I(n) = I(n - 15) \oplus I(n - 13) \oplus I(n - 9) \oplus I(n - 8) \oplus I(n - 7) \oplus I(n - 5)$$

16 (based on  $P_I(x)$  as the characteristic polynomial)

17 and

18 
$$Q(n) = Q(n - 15) \oplus Q(n - 12) \oplus Q(n - 11) \oplus Q(n - 10) \oplus Q(n - 6) \oplus Q(n - 5) \oplus$$
  
19 
$$Q(n - 4) \oplus Q(n - 3)$$

20 (based on  $P_Q(x)$  as the characteristic polynomial),

21 where  $I(n)$  and  $Q(n)$  are binary valued ('0' and '1') and the additions are modulo-2. In order  
22 to obtain the I and Q pilot PN sequences (of period  $2^{15}$ ), a '0' is inserted in the  $\{I(n)\}$  and  
23  $\{Q(n)\}$  sequences after 14 consecutive '0' outputs (this occurs only once in each period).  
24 Therefore, the pilot PN sequences have one run of 15 consecutive '0' outputs instead of 14.

1 The chip rate for the pilot PN sequence shall be 1.2288 Mcps. The pilot PN sequence period  
2 is  $32768/1228800 = 26.666\dots$  ms, and exactly 75 pilot PN sequence repetitions occur every  
3 2 seconds.

4 Pilot Channels shall be identified by an offset index in the range from 0 through 511  
5 inclusive. This offset index shall specify the offset value (in units of 64 chips) by which the  
6 pilot PN sequence lags the zero-offset pilot PN sequence. The zero-offset pilot PN sequence  
7 shall be such that the start of the sequence shall be output at the beginning of every even  
8 second in time, referenced to access network transmission time. The start of the zero-offset  
9 pilot PN sequence for either the I or Q sequences shall be defined as the state of the  
10 sequence for which the next 15 outputs inclusive are '0'. Equivalently, the zero-offset  
11 sequence is defined such that the last chip prior to the even-second mark as referenced to  
12 the transmit time reference is a '1' prior to the 15 consecutive '0's.

### 13 1.4.1.3.5 Filtering

#### 14 1.4.1.3.5.1 Baseband Filtering

15 Following the quadrature spreading operation, the I' and Q' impulses are applied to the  
16 inputs of the I and Q baseband filters as shown in Figure 1.4.1.3.1-1. The baseband filters  
17 shall have a frequency response  $S(f)$  that satisfies the limits given in Figure 1.4.1.3.5.1-1.  
18 Specifically, the normalized frequency response of the filter shall be contained within  $\pm\delta_1$  in  
19 the passband  $0 \leq f \leq f_p$  and shall be less than or equal to  $-\delta_2$  in the stopband  $f \geq f_s$ . The  
20 numerical values for the parameters are  $\delta_1 = 1.5$  dB,  $\delta_2 = 40$  dB,  $f_p = 590$  kHz, and  $f_s = 740$   
21 kHz.

22



1

**Table 1.4.1.3.5.1-1. Baseband Filter Coefficients**

<b>k</b>	<b>h(k)</b>
0, 47	-0.025288315
1, 46	-0.034167931
2, 45	-0.035752323
3, 44	-0.016733702
4, 43	0.021602514
5, 42	0.064938487
6, 41	0.091002137
7, 40	0.081894974
8, 39	0.037071157
9, 38	-0.021998074
10, 37	-0.060716277
11, 36	-0.051178658
12, 35	0.007874526
13, 34	0.084368728
14, 33	0.126869306
15, 32	0.094528345
16, 31	-0.012839661
17, 30	-0.143477028
18, 29	-0.211829088
19, 28	-0.140513128
20, 27	0.094601918
21, 26	0.441387140
22, 25	0.785875640
23, 24	1.0

2

## 3 1.4.1.3.5.2 Phase Characteristics

4 The access network shall provide phase equalization for the transmit signal path.<sup>9</sup> The  
5 equalizing filter shall be designed to provide the equivalent baseband transfer function

$$H(\omega) = K \frac{\omega^2 + j\alpha\omega\omega_0 - \omega_0^2}{\omega^2 - j\alpha\omega\omega_0 - \omega_0^2},$$

6

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<sup>9</sup>This equalization simplifies the design of the access terminal receive filters.

1 where  $K$  is an arbitrary gain,  $j$  equals  $\sqrt{-1}$ ,  $\alpha$  equals 1.36,  $\omega_0$  equals  $2\pi \times 3.15 \times 10^5$ , and  $\omega$   
 2 is the radian frequency. The equalizing filter implementation shall be equivalent to applying  
 3 baseband filters with this transfer function, individually, to the baseband I and Q  
 4 waveforms.

5 A phase error test filter is defined to be the overall access network transmitter filter  
 6 (including the equalizing filter) cascaded with a filter having a transfer function that is the  
 7 inverse of the equalizing filter specified above. The response of the test filter should have a  
 8 mean squared phase error from the best fit linear phase response that is no greater than  
 9 0.01 squared radians when integrated over the frequency range  $1 \text{ kHz} \leq |f - f_c| \leq 630 \text{ kHz}$ .  
 10 For purposes of this requirement, "overall" shall mean from the I and Q baseband filter  
 11 inputs (see Table 1.4.1.3.5.1-1) to the RF output of the transmitter.

#### 12 1.4.1.3.6 Synchronization and Timing

##### 13 1.4.1.3.6.1 Timing Reference Source

14 Each sector shall use a time base reference from which all time-critical transmission  
 15 components, including pilot PN sequences, slots, and Walsh functions, shall be derived.  
 16 The time-base reference shall be time-aligned to CDMA System Time, as described in Figure  
 17 1.14-1 of [1]. Reliable external means should be provided at each sector to synchronize  
 18 each sector's time base reference to CDMA System Time. Each sector should use a  
 19 frequency reference of sufficient accuracy to maintain time alignment to CDMA System  
 20 Time. In the event that the external source of CDMA System Time is lost,<sup>10</sup> the sector shall  
 21 maintain transmit timing within  $\pm 10 \mu\text{s}$  of CDMA System Time for a period of not less than  
 22 8 hours.

##### 23 1.4.1.3.6.2 Sector Transmission Time

24 All sectors should radiate the pilot PN sequence within  $\pm 3 \mu\text{s}$  of CDMA System Time and  
 25 shall radiate the pilot PN sequence within  $\pm 10 \mu\text{s}$  of CDMA System Time.

26 Time measurements are made at the sector antenna connector. If a sector has multiple  
 27 radiating antenna connectors for the same CDMA channel, time measurements are made at  
 28 the antenna connector having the earliest radiated signal.

29 The rate of change for timing corrections shall not exceed 102 ns (1/8 PN chip) per 200 ms.  
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<sup>10</sup> These guidelines on time keeping requirements reflect the fact that the amount of time error between sectors that can be tolerated in an access network is not a hard limit. Each access terminal can search an ever-increasing time window as directed by the sectors. However, increasing this window gradually degrades performance since wider windows require a longer time for the access terminals to search out and locate the various arrivals from all sectors that may be in view.

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